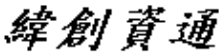


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Schematics Document

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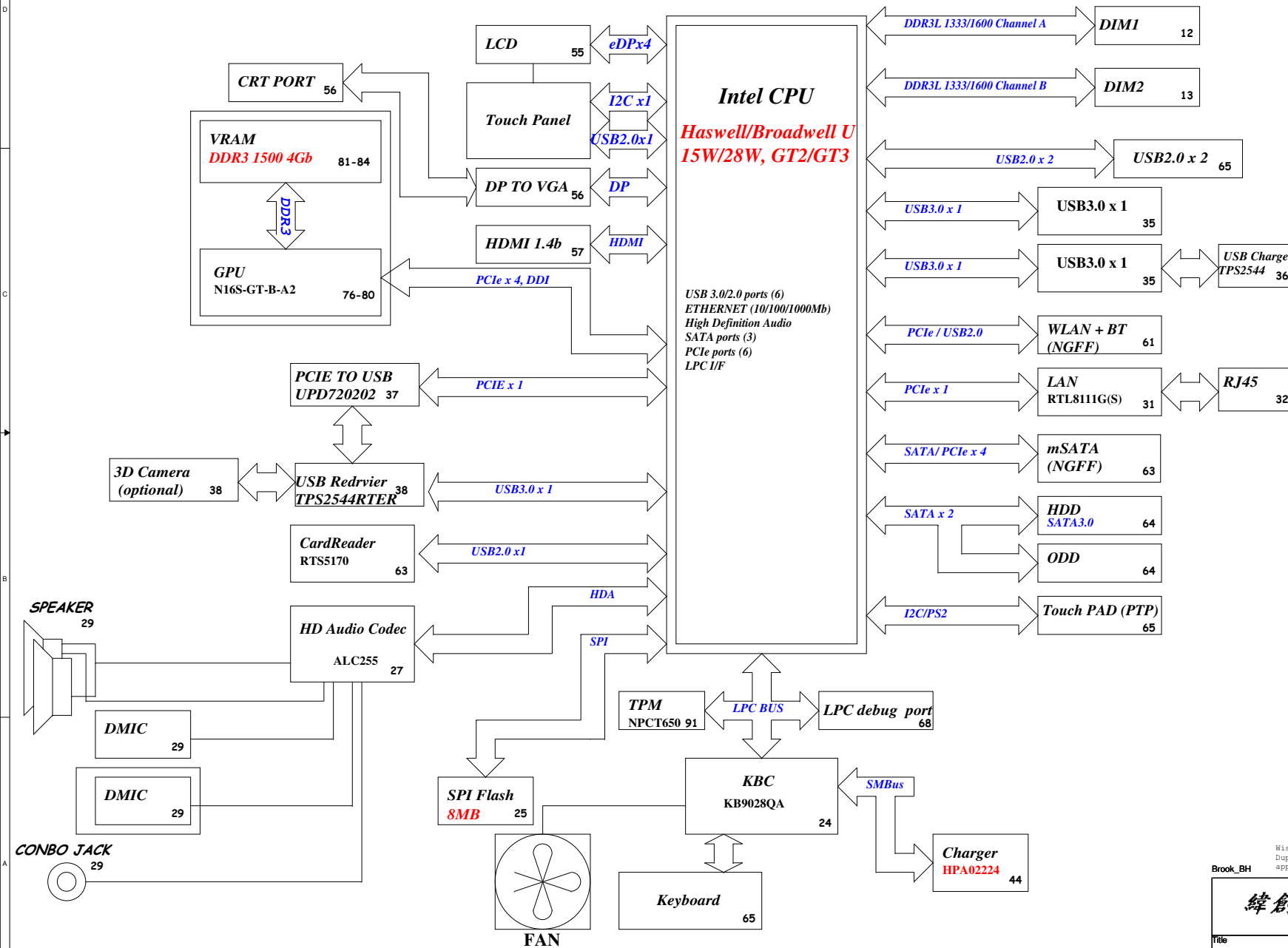
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover Page			
Size A4	Document Number Brook_BH		Rev -1M
Date: Wednesday, February 04, 2015	Sheet	1 of	106

BROOK ULT Board Block Diagram

Project code : 4PD04X010001

PCB P/N : 14276

Revision : -1M

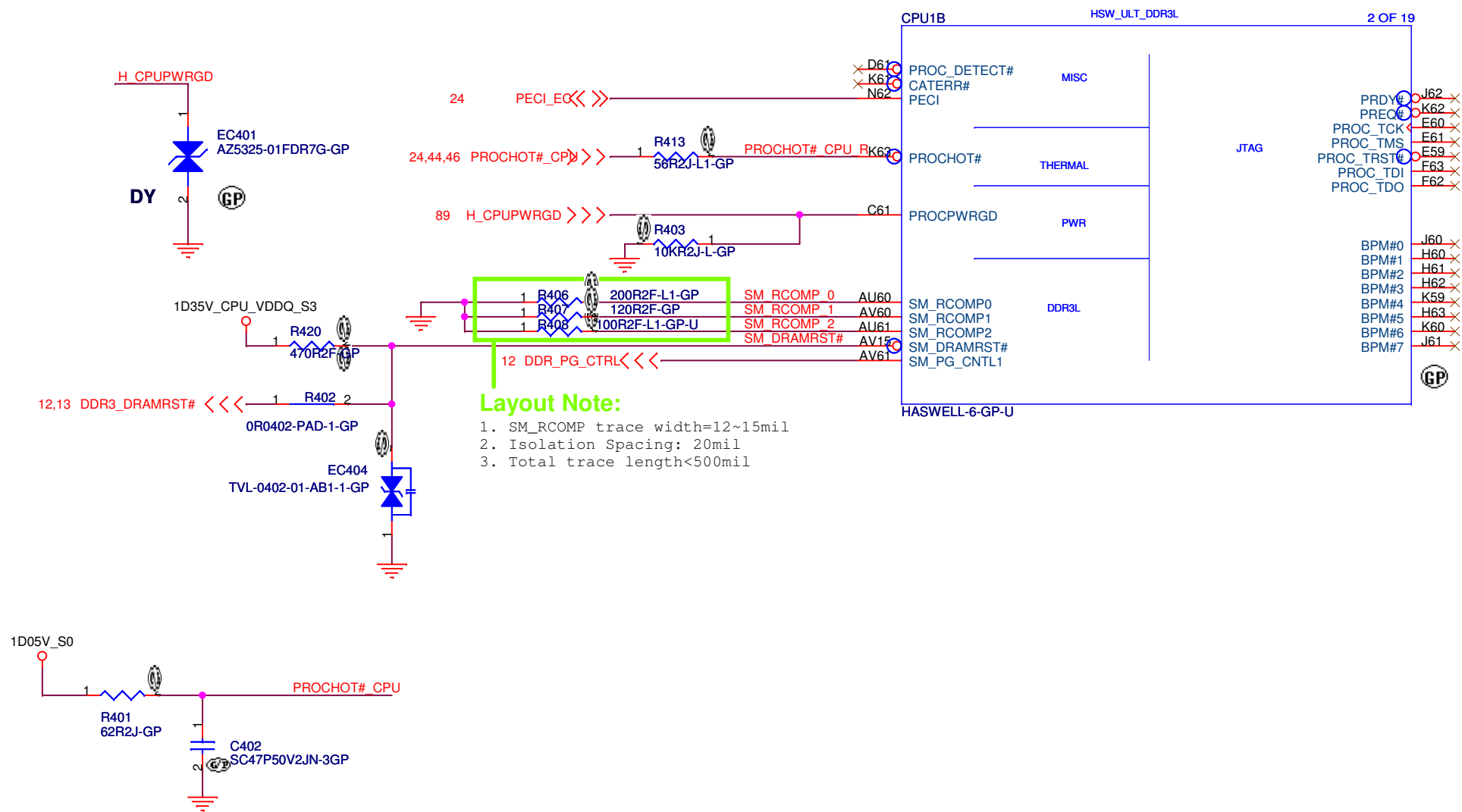


CHARGER	HPA02224	44
INPUTS	OUTPUTS	
DCBATOUT	BT+	
SYSTEM DC/DC	RT6575B	45
INPUTS	OUTPUTS	
DCBATOUT	5V_S5 3D3V_S5	
CPU DC/DC	RT6575B	46-47
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
SYSTEM DC/DC	TPS51716	48
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	
SYSTEM DC/DC	RT8231	49
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3	
SYSTEM LDO	S13390D15	51
INPUTS	OUTPUTS	
3D3V_S5	1D3V_S5	

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Title

CPU (THERMAL/CLOCK/PM)

Size
A4

Document Number

Brook BH

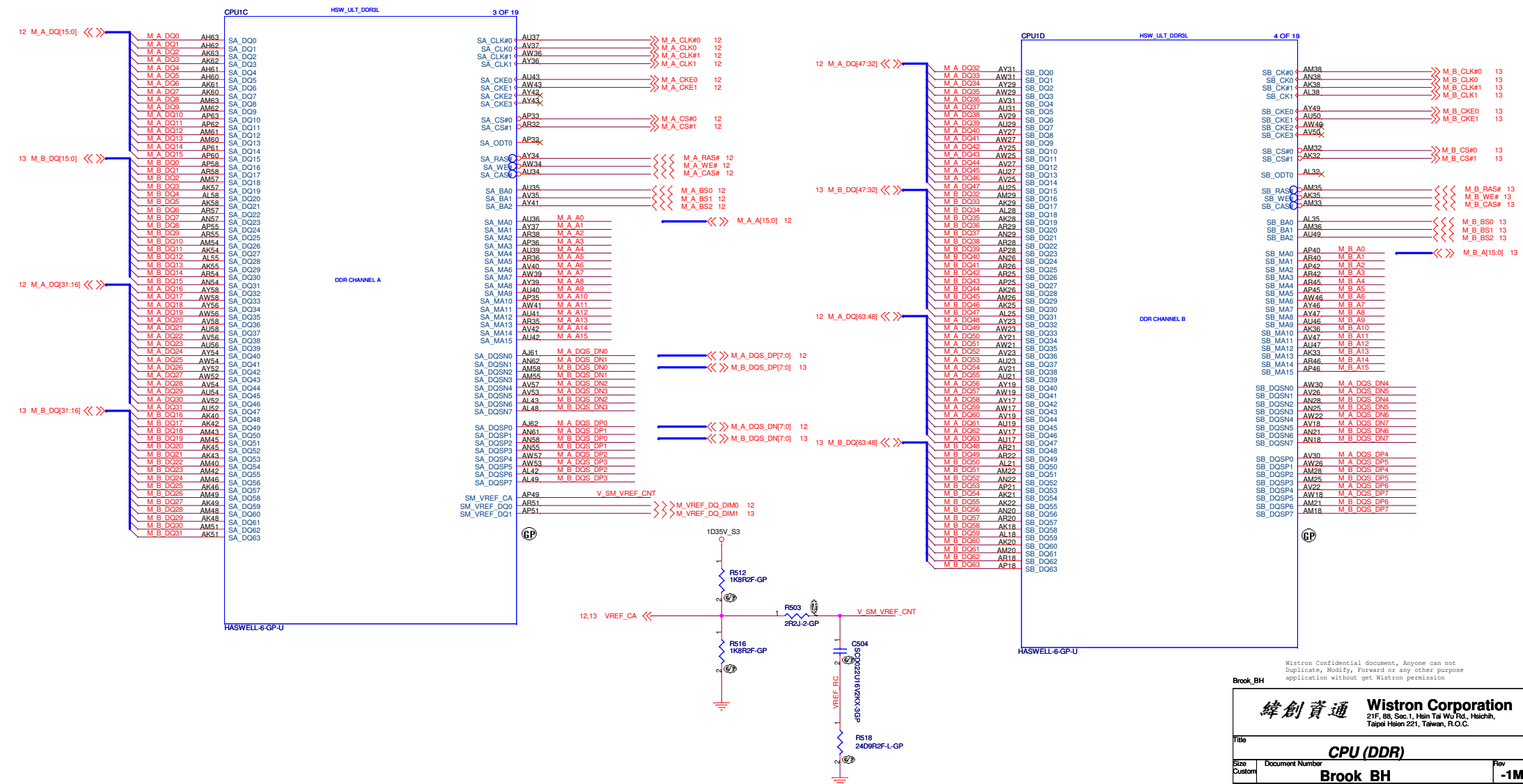
Rev

-1M

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Sheet 4 of 106

SSID = CPU



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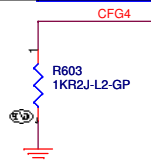
Title			
CPU (DDR)			
Size	Document Number	Rev	
Custom	Brook BH	-1M	
Date:	Wednesday, February 04, 2015	Sheet	5 of 106

SSID = CPU

Pin Name	System Pull-up/Pull-down	Schematic Notes	✓
CFG[19:0]		Please refer to the <i>Crescent Bay and (??) Platforms - Debug Port Design Guide (DPDG)</i> .	

Note: Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

eDP Enable	
CFG4	1:Disable 0:Enable



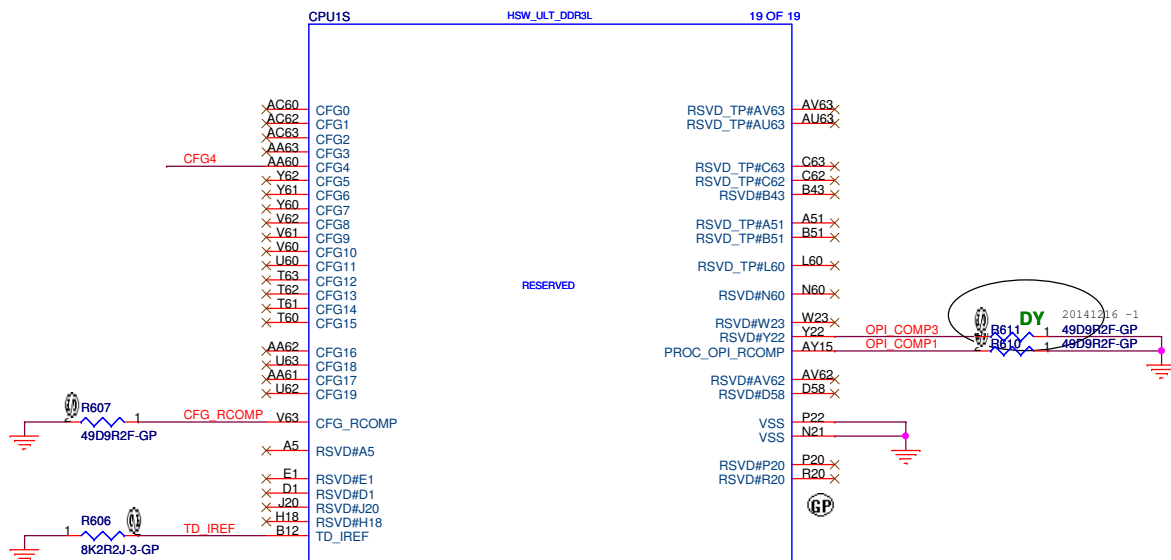
Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none">• CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.• PCI Express* Static x16 Lane Numbering Reversal.——• CFG[4]: eDP enable<ul style="list-style-type: none">— 1 = Disabled— 0 = Enabled• [19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left un-connected

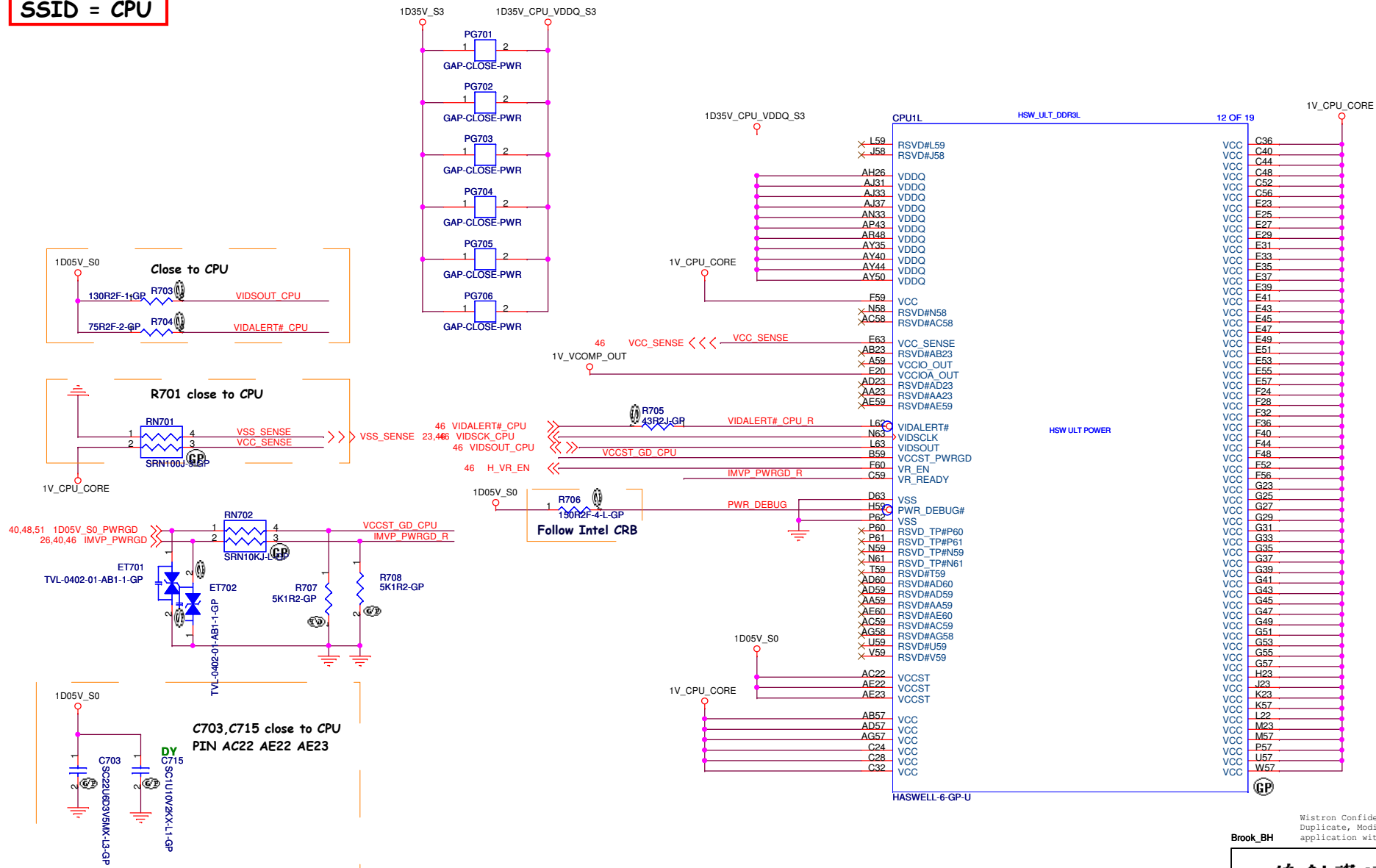


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Date:	Wednesday, February 04, 2015	Sheet	6 of 106

SSID = CPU



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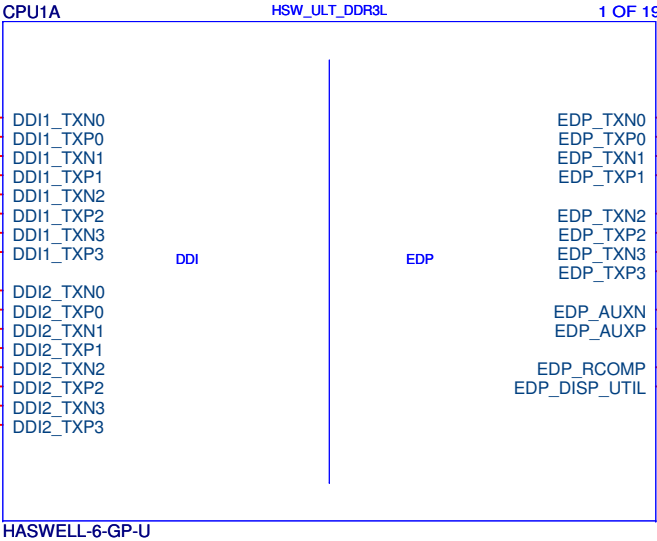
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CPU (VCC CORE)		
Size	Document Number	Rev
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Date:	Wednesday, February 04, 2015	Sheet 7 of 106

SSID = CPU

HDMI

DP to Display Port



eDP

eDP x4 reserve

Layout Note:

Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

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CPU (DDI/EDP)

Size

A4

Document Number

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Rev

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Date:

Wednesday, February 04, 2015

Sheet

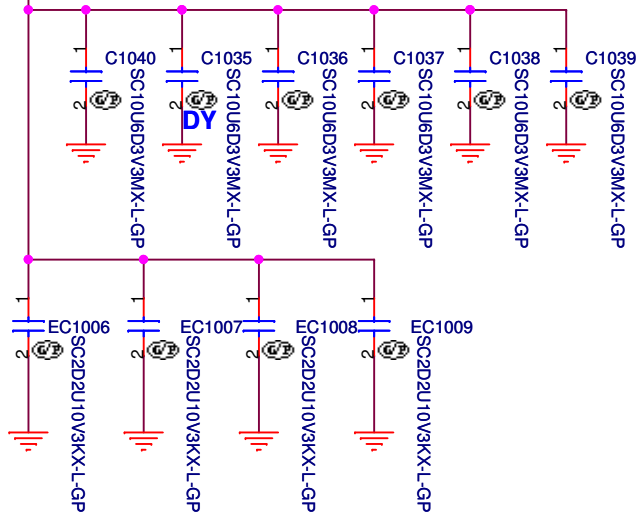
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of

106

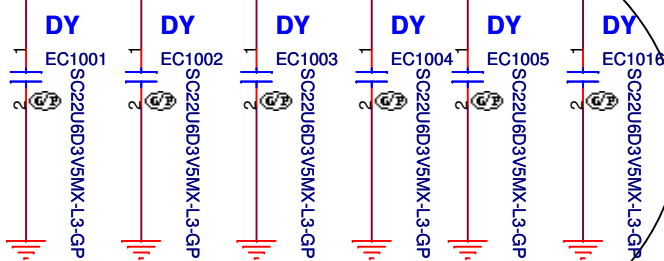
1D35V_CPU_VDDQ_S3

Power current=3A



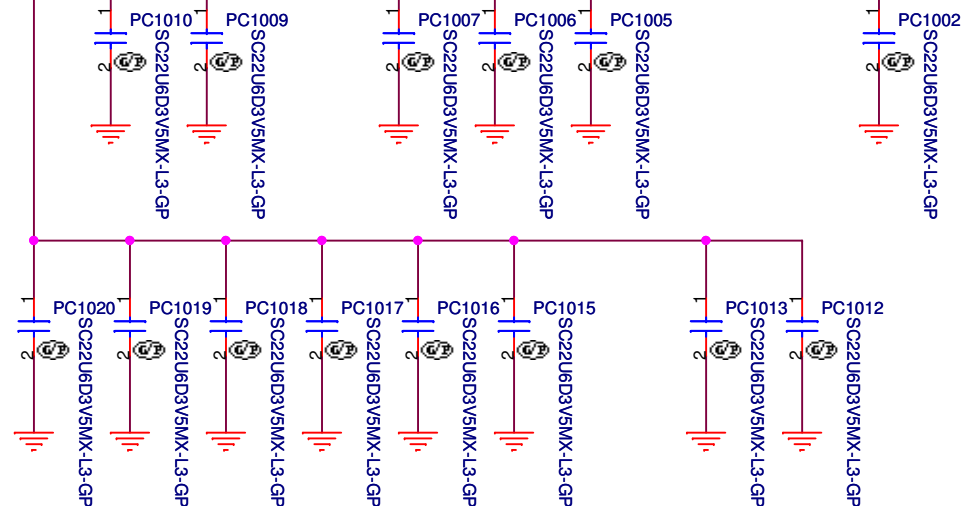
For Intel Recommend EE Part

1V_CPU_CORE

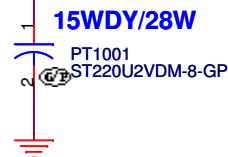


1V_CPU_CORE

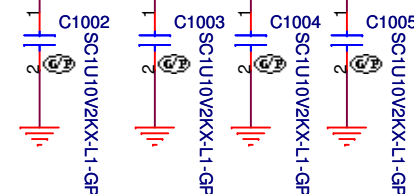
Power current=40A



1V_CPU_CORE



1V_CPU_CORE



For Intel Recommend EE Part

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Title

CPU (Power CAP1)

Size
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Document Number

Brook BH

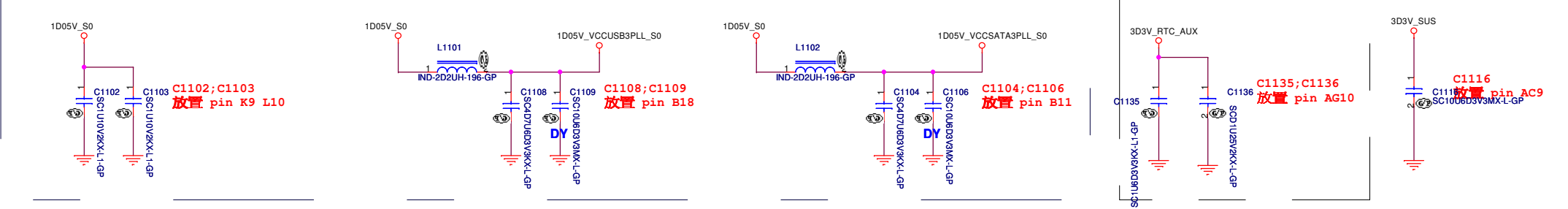
Rev
-1M

Date: Wednesday, February 04, 2015

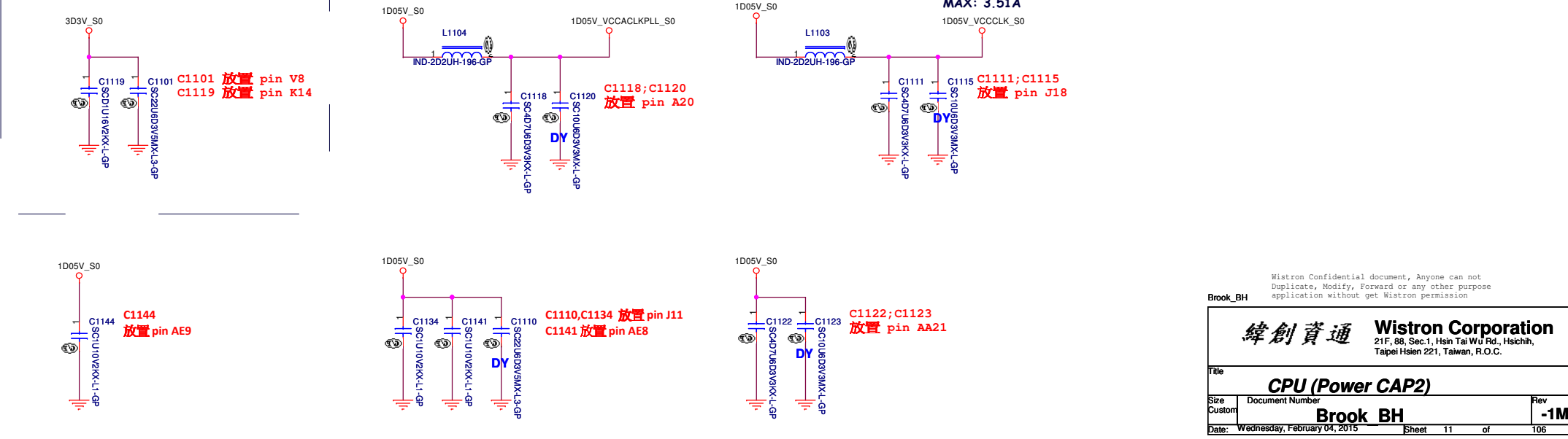
Sheet 10 of 106

擺放電容的位置請參考 Page 21, 每個位置如下

MAX: 3.074A



MAX: 0.285A

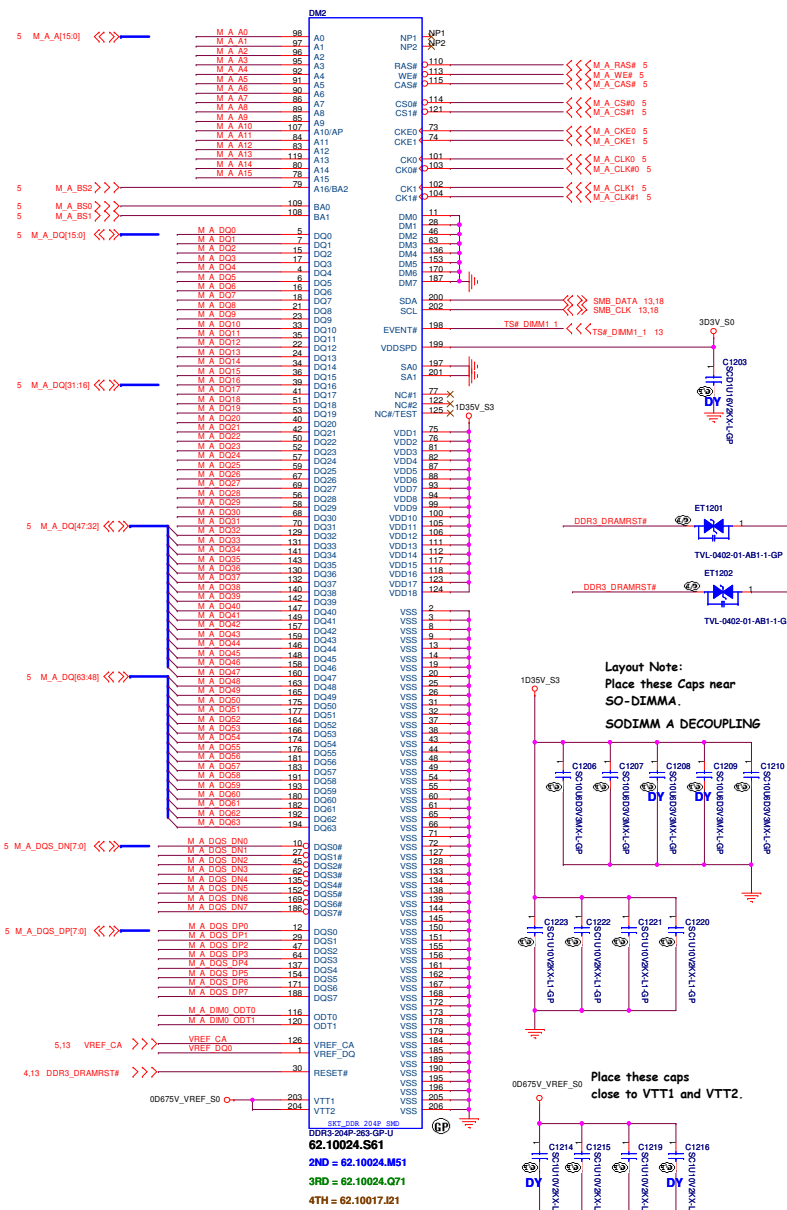


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Title		
CPU (Power CAP2)		
Size	Document Number	Rev
Custom	Brook BH	-1M
Date: Wednesday, February 04, 2015	Sheet 11 of 106	

SSID = MEMORY



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

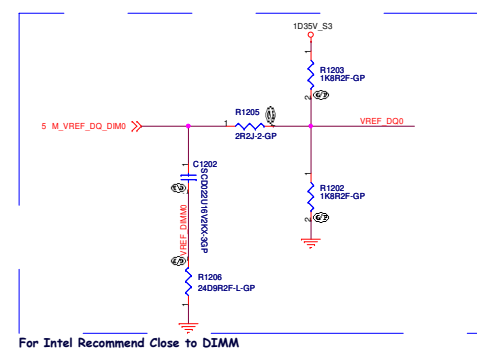
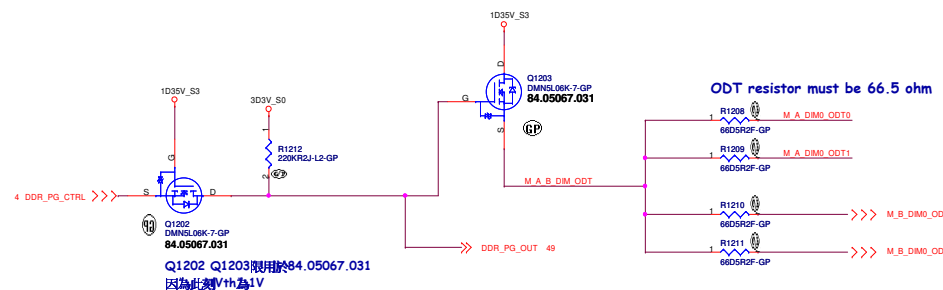
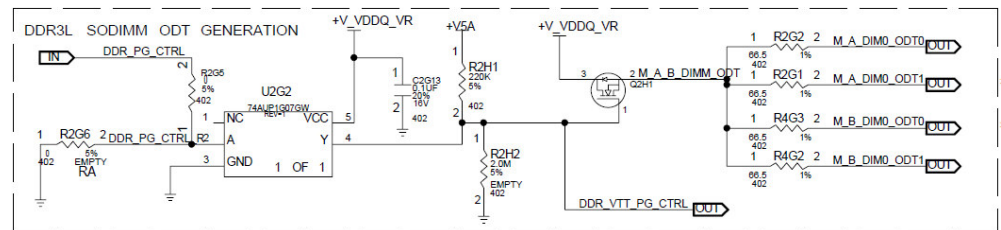
SODIMM Memory Connectivity and Topology

ODT Signal Connectivity and Support

For DDR3L SODIMM designs, Intel recommends ODT signals not to be routed between CPU and DIMM on platform, leave ODT at CPU as no-connect (open), and tie DIMM ODT to VDDQ through FET and resistor. The reason for this additional ODT-control circuitry on the platform is to save power dissipation by turning off VDDQ to VTT path during low power states, as ODT signal is terminated to VTT through RTT on SODIMM. The ODT value for DDR3L SODIMM 1-DPC platform will be encoded in the write command and use RTT_NOM = Off and RTT_WR = (60,120) Ohm.

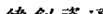
- CPU ODT output would be NOCON

- SODIMM ODT input should be tied to VDDQ through a FET and a resistor to support low power states.

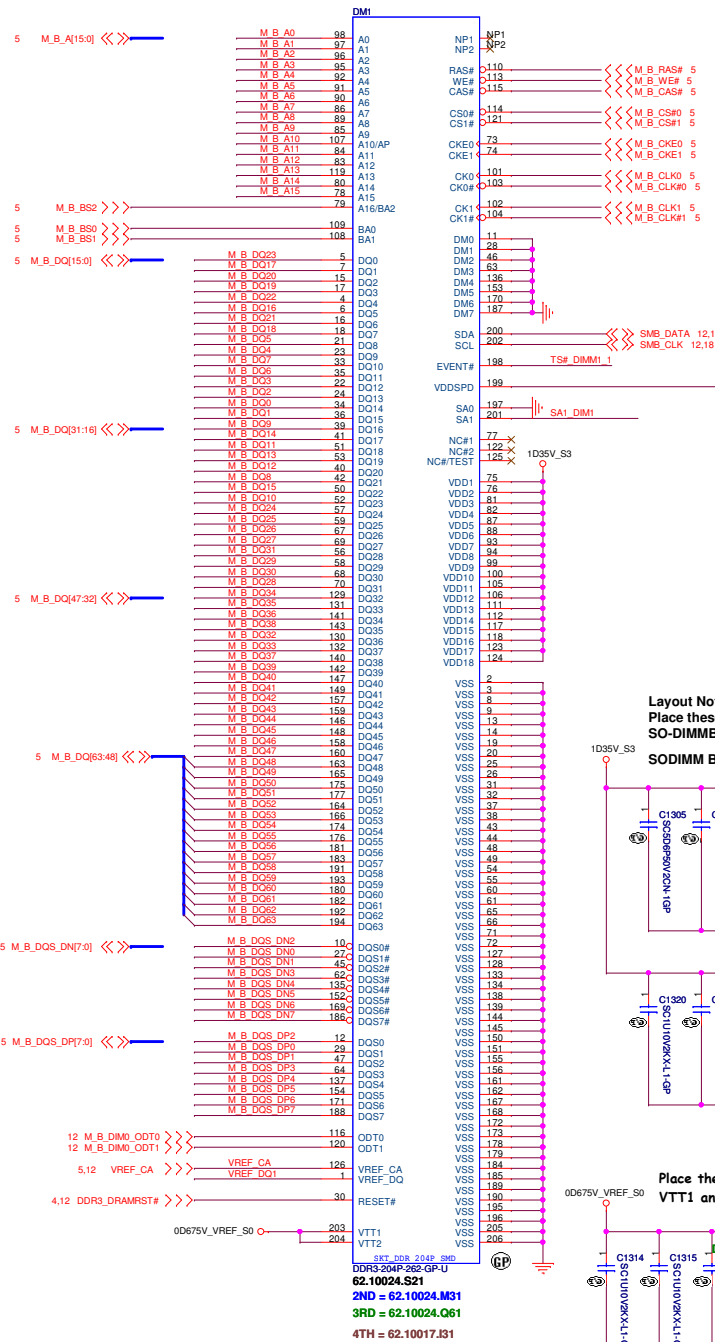


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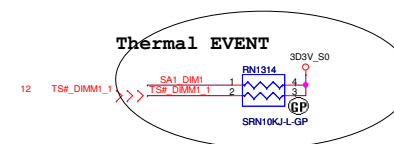
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Title			
DDR3-SODIMM1			
Size A2	Document Number	Brook BH	Rev -1M
Date:	Wednesday, February 04, 2015	Sheet 12 of	106

SSID = MEMORY



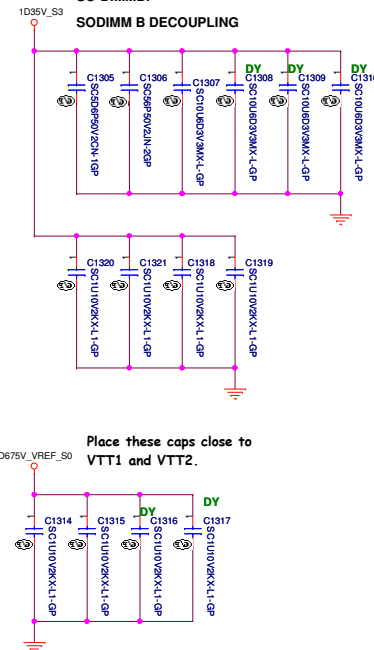
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

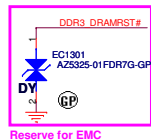
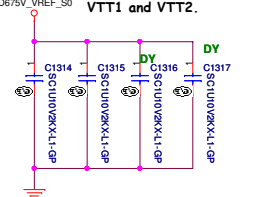


Layout Note:
Place these Caps near
SO-DIMMB.

SODIMM B DECOUPLING

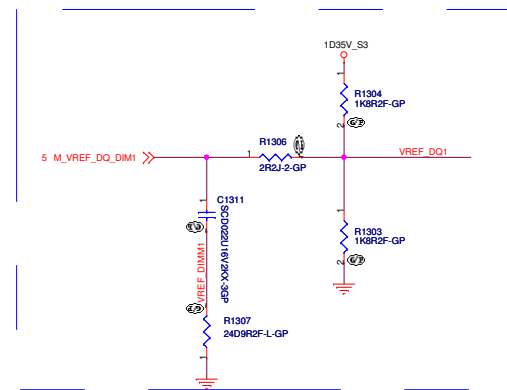
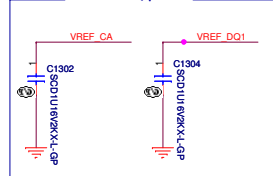


Place these caps close to
VTT1 and VTT2.



Reserve for EMC

Close RAM3 CA & DQ pin



For Intel Recommend Close to DIMM

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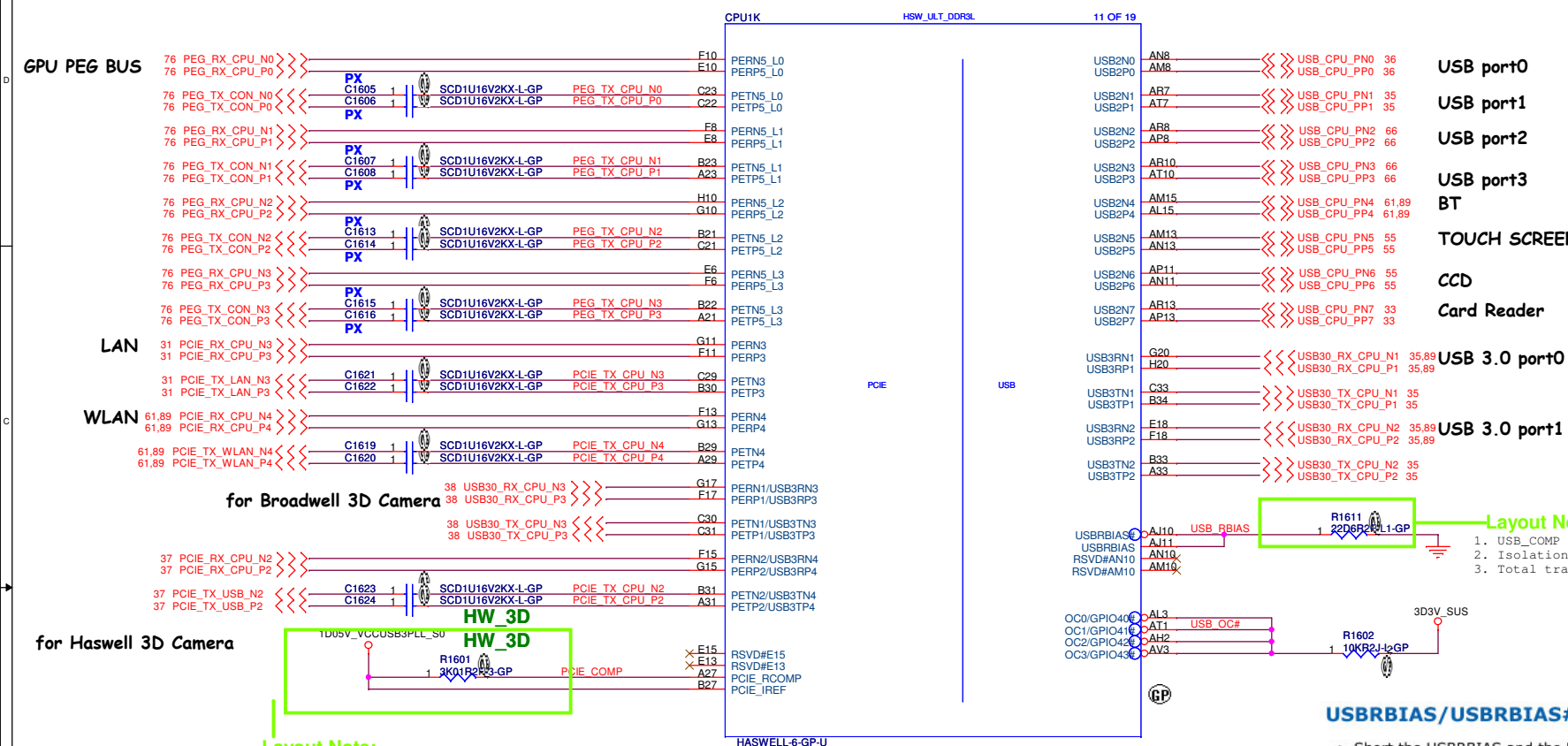
DDR3-SODIMM2

Size Custom	Document Number Brook BH	Rev 1
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Date: Wednesday, February 04, 2015 Sheet 13 of 106

USB Table

Pair	Device
0	USB3.0 Port0
1	USB3.0 Port1
2	USB3.0 Port2
3	USB3.0 Port3
4	BT
5	TOUCH SCREEN
6	CCD
7	Card Reader



USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω $\pm 1\%$ resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

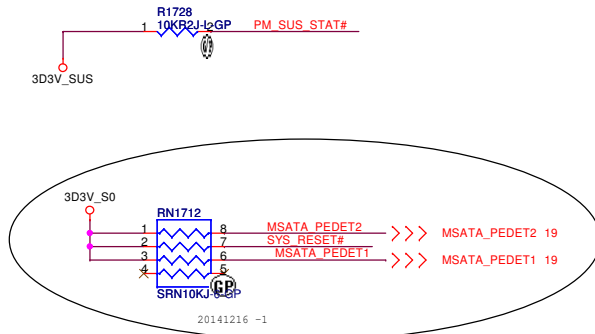
Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm $\pm 1\%$ pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

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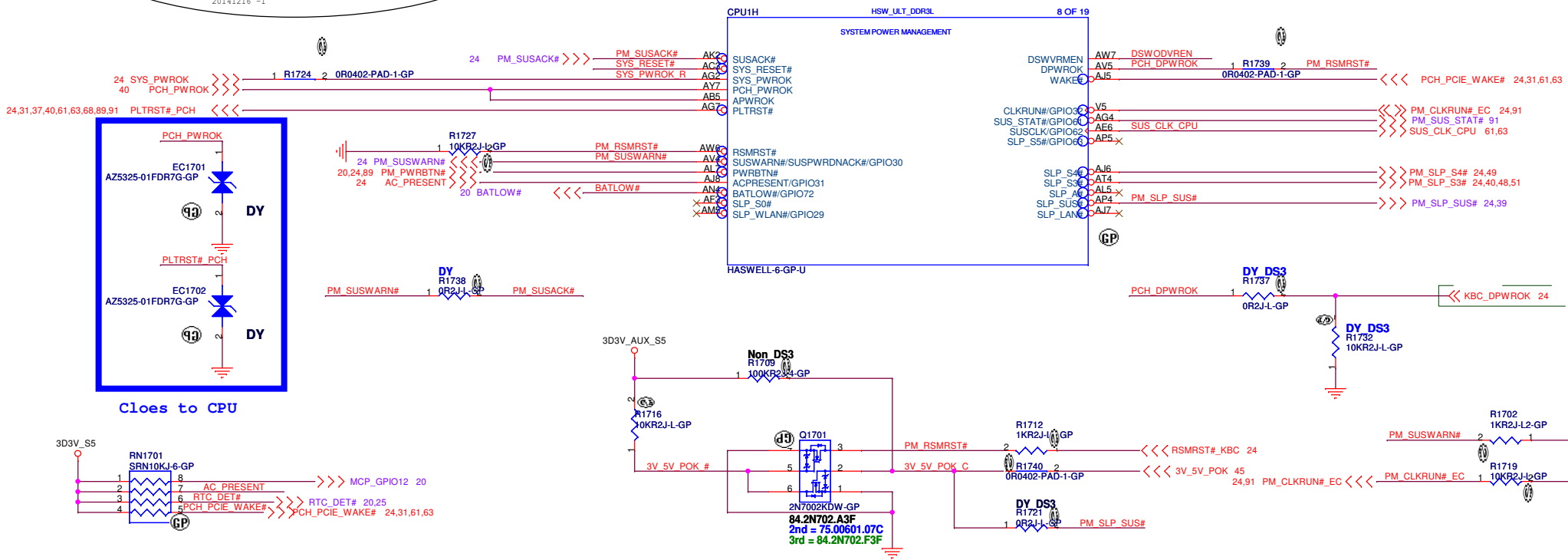
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Title			CPU (PCI/USB)	
Size	Document Number	Rev		
A3		Brook BH		-1M
Date:	Wednesday, February 04, 2015	Sheet	16	of 106

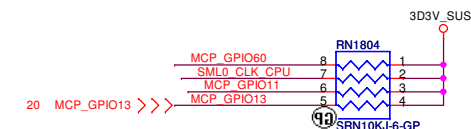
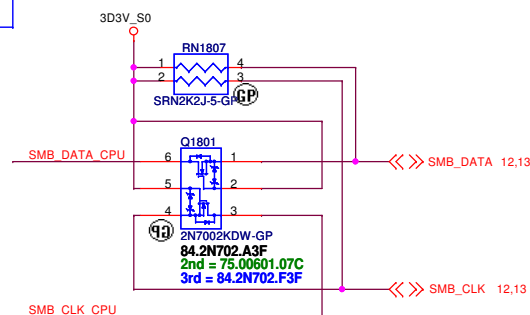
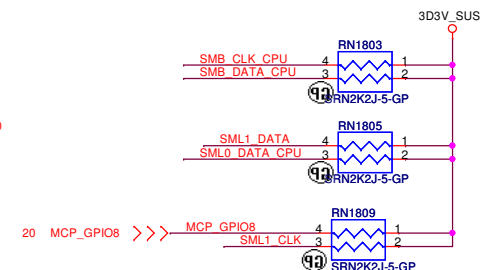
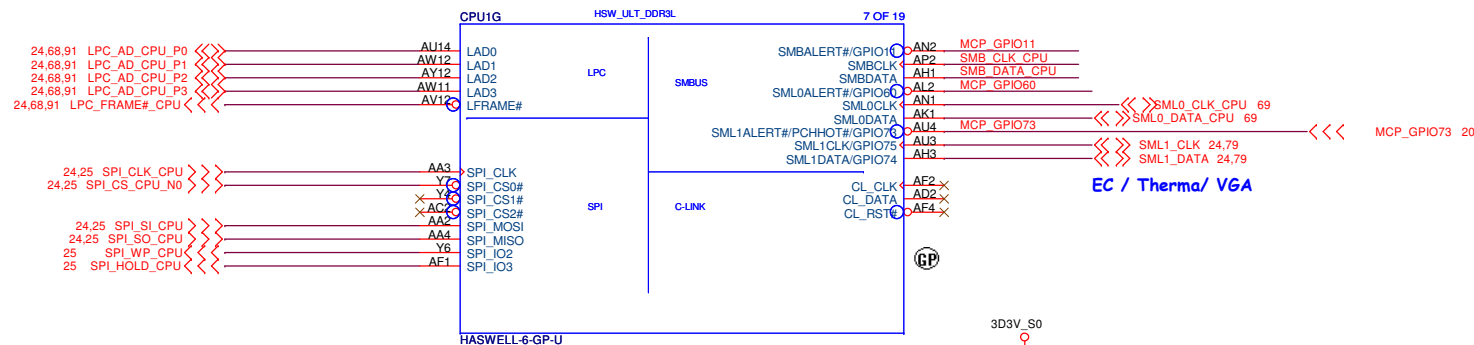
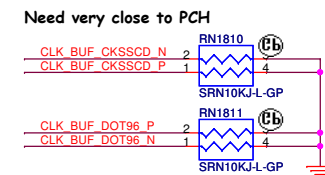
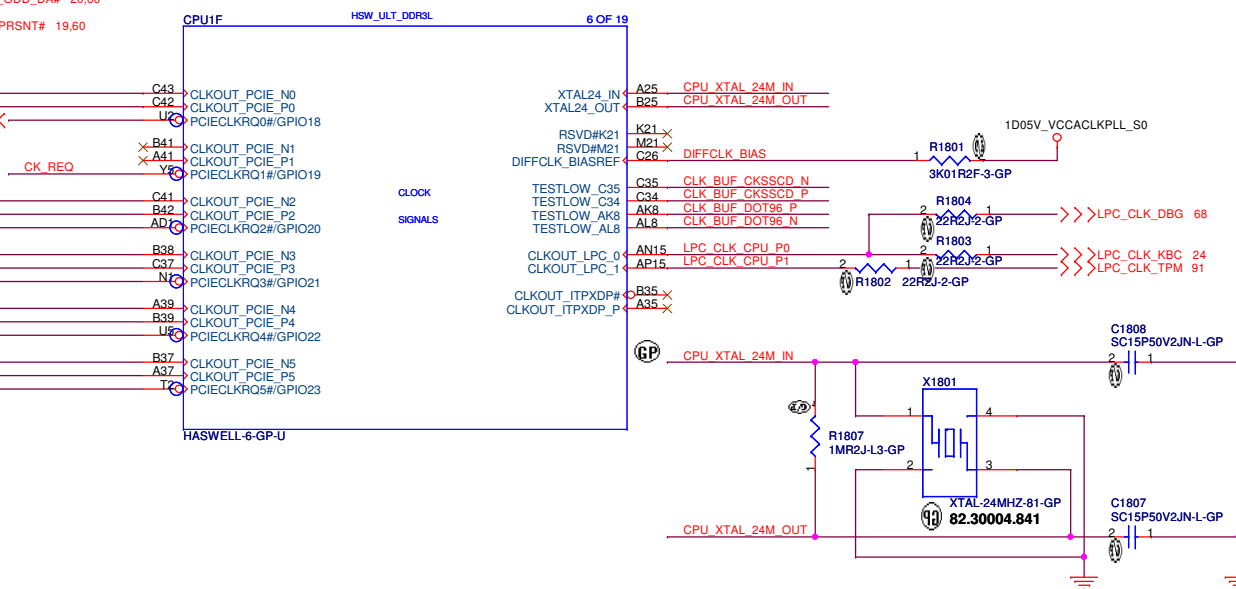
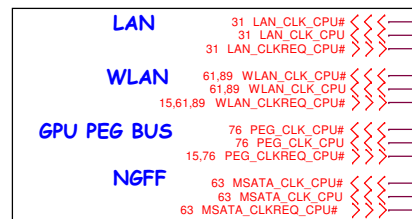
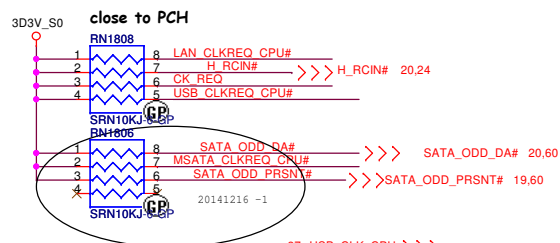


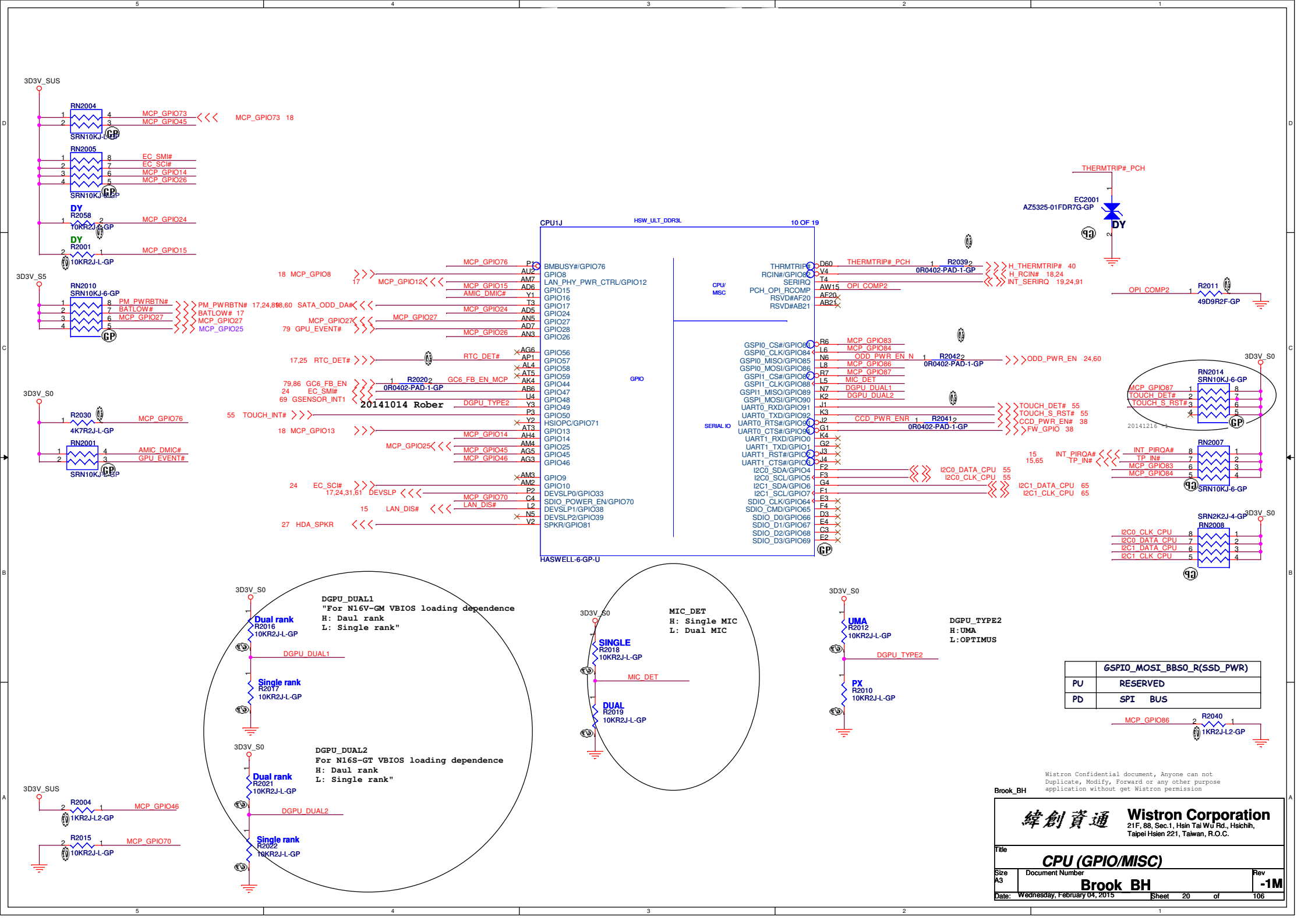
Bit	Description
31:3	Reserved
2	<p>WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case).</p> <p>When this bit is '0':</p> <ul style="list-style-type: none"> Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. <p>NOTE: Deep Sx disabled configuration must leave this bit at '0'.</p>

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



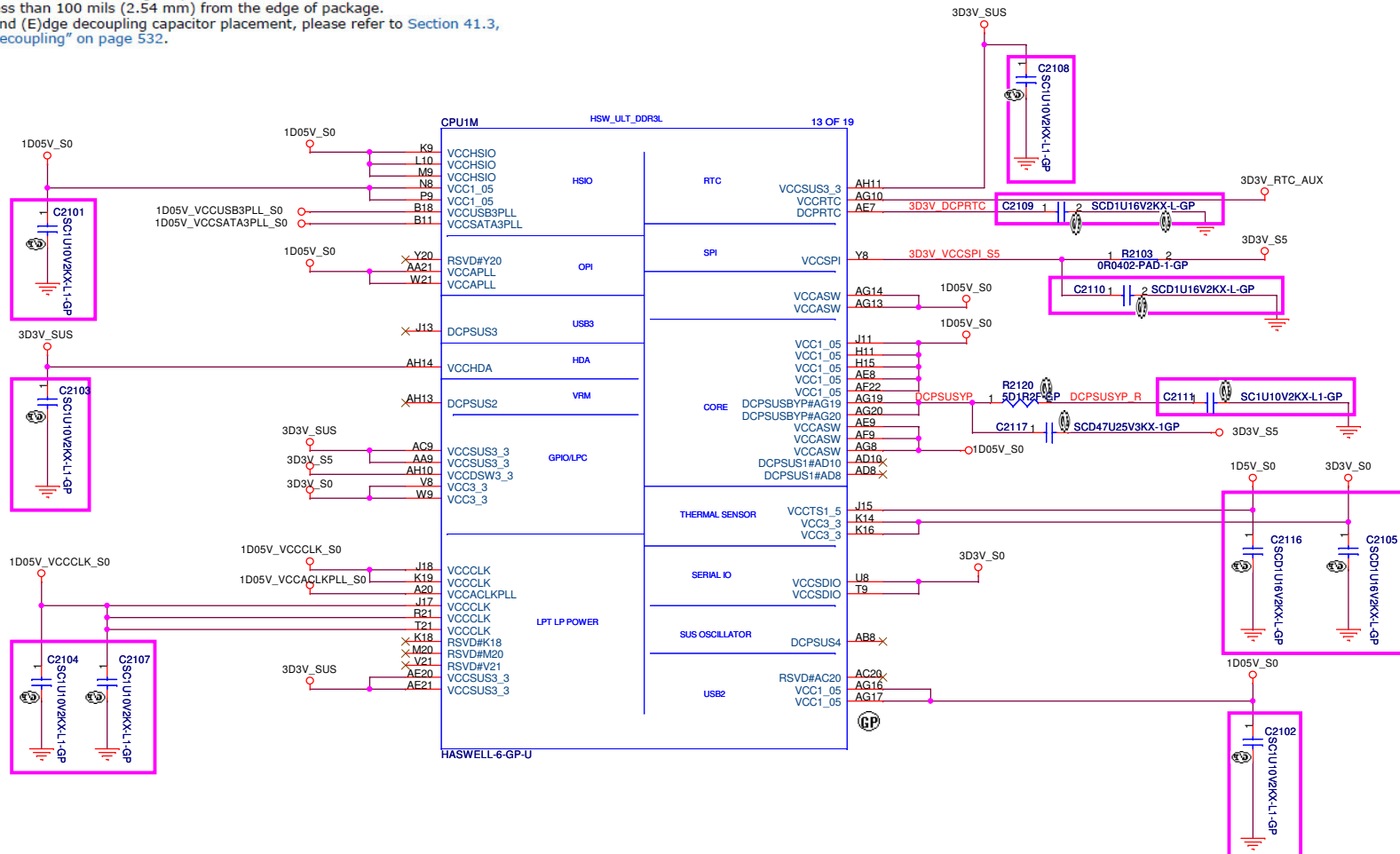
Closes to CPU





Notes:

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3](#), "Loop Inductance Reduction Decoupling" on page 532.



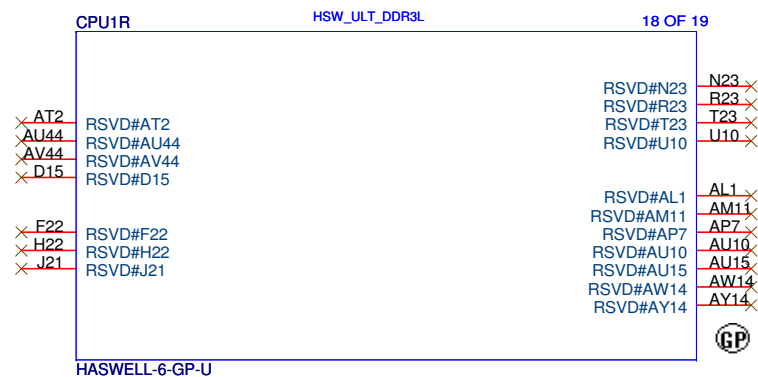
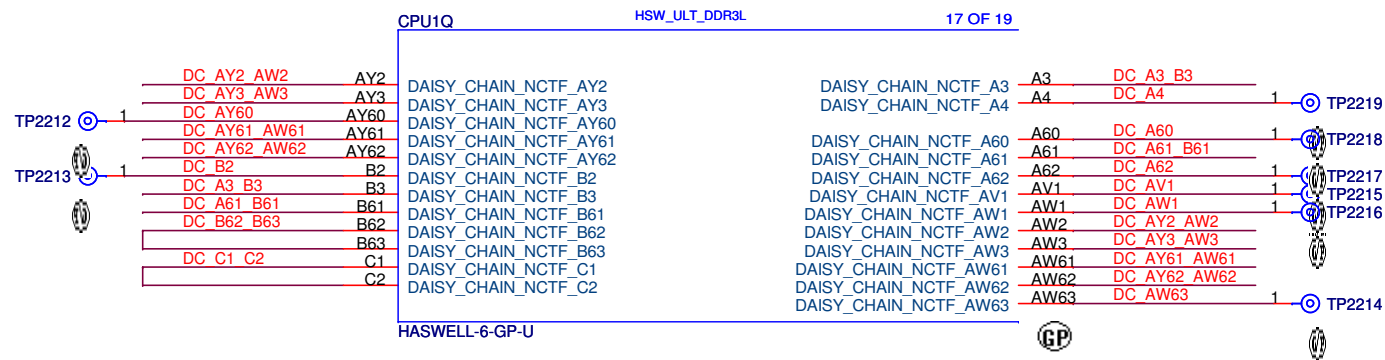
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CPU (POWER1)		
Size	Document Number	Rev
A3		-1M
Date:	Wednesday, February 04, 2015	Sheet 21 of 106

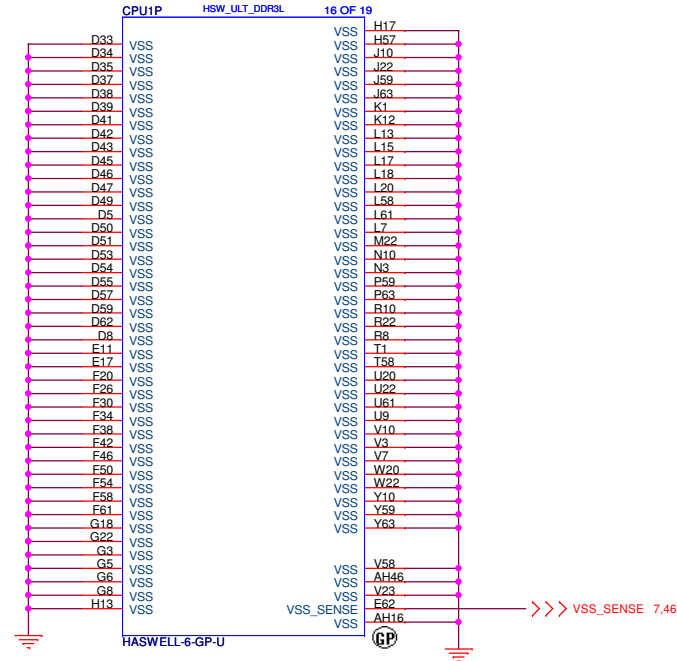
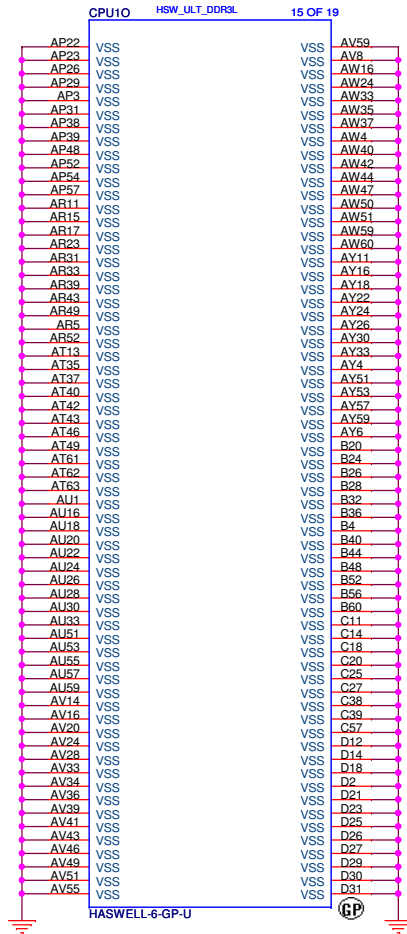
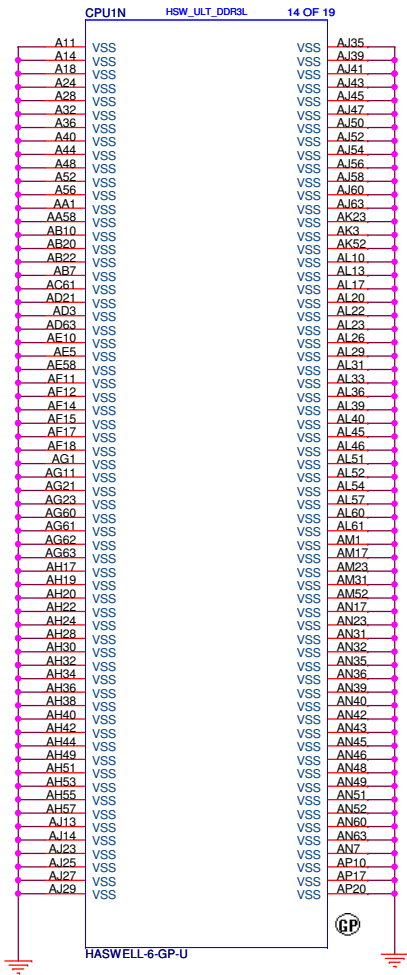
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CPU (RSVD)			
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Title		CPU (VSS)	
Size	Document Number	Rev	
A3	Brook BH	-1M	
Date:	Wednesday, February 04, 2015	Sheet	23 of 106

SSID = Flash.ROM

SPI FLASH ROM (32K b,ts) for PCH

SPI ROM Equal length need to less than 500mil

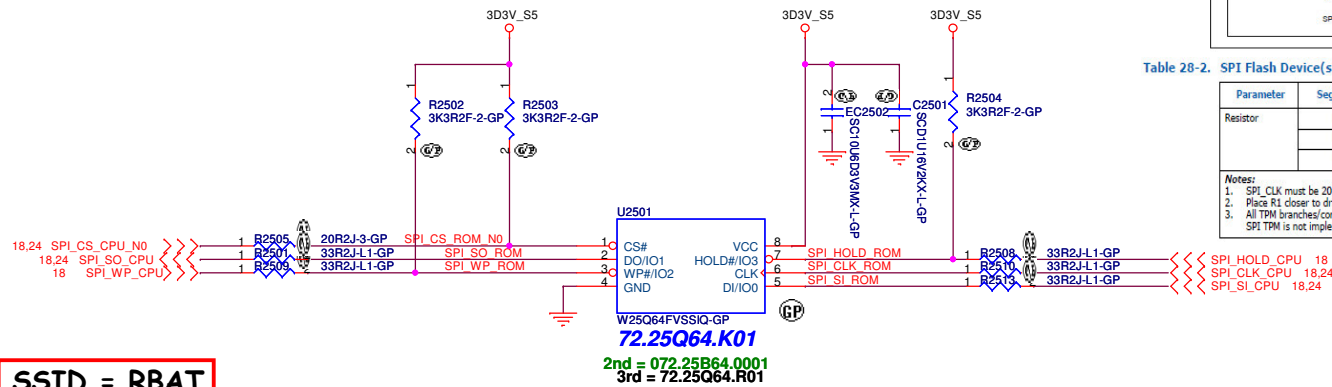
SPI FLASH ROM (8M byte)

1ST= 072.02564.0001 (AMIC A25LQ64M)

2ND=072.25B64.0001 (Gigadevice GD25B64BSIGR)

purge=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)

72.25647.00A (MXIC MX25L6473EM2I)



SSID = RBAT

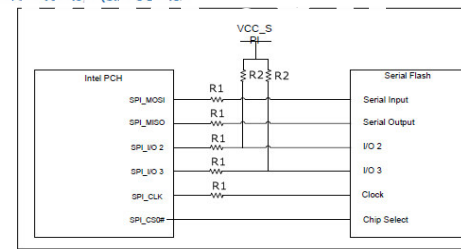
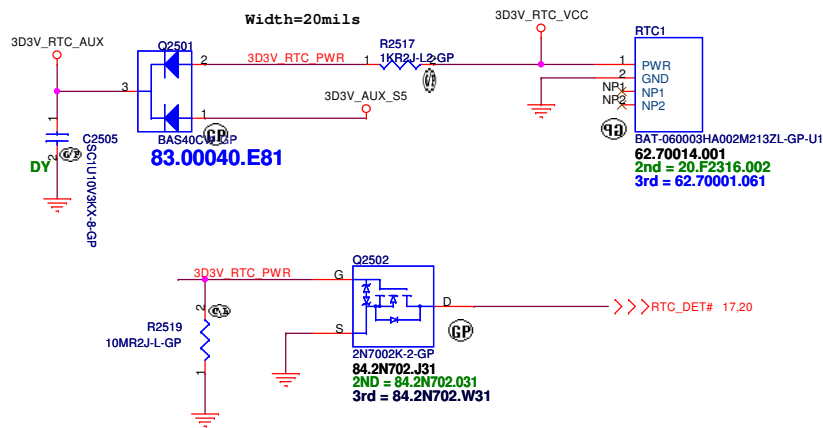


Table 28-2. SPI Flash Device(s) and TPM Routing Guideline (Sheet 2 of 2)

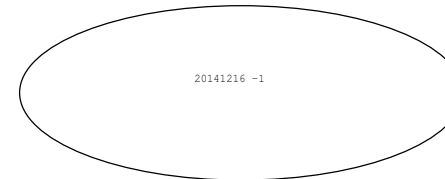
Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

Notes:

- SPL_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
- Place R1 closer to driver side to effectively damping the underhoot and overshoot.
- All TPM branches/connections (TPM_MOST, TPM_MISO, TPM_CLK, and PCH_CS2*) can be left as NC. SPI TPM is not implemented.

Notes:

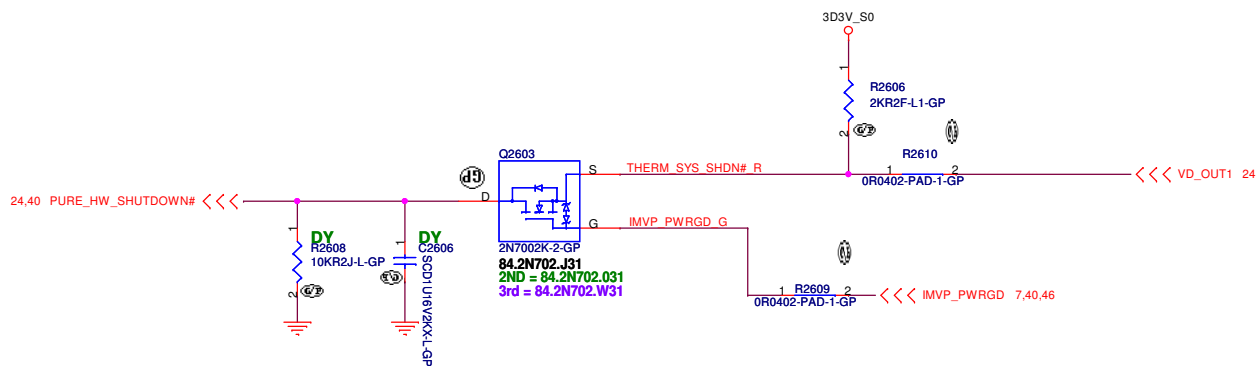
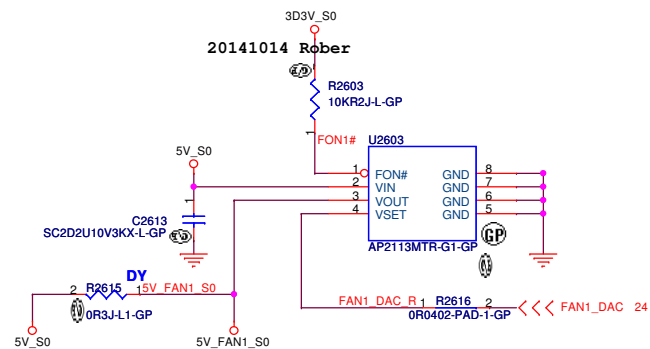
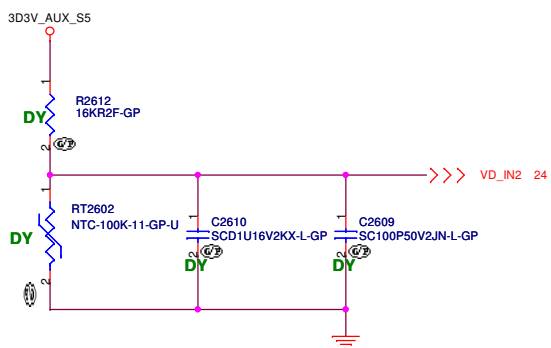
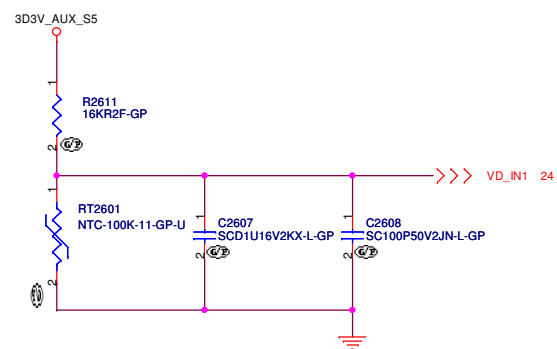
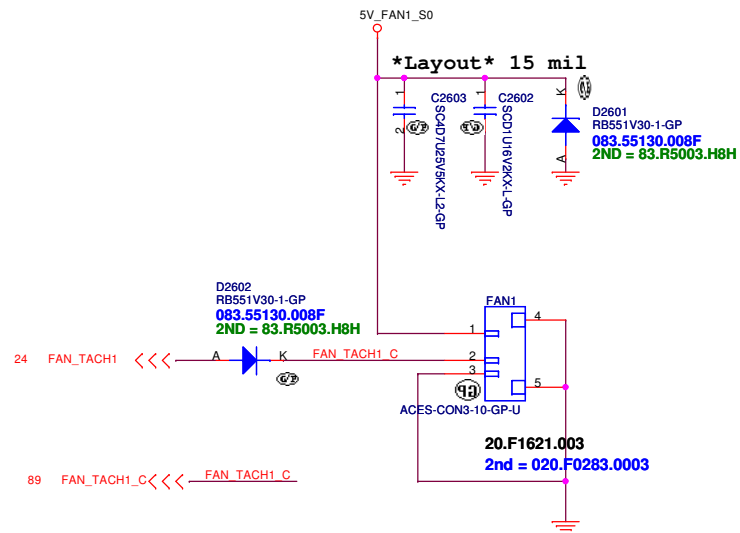
1. SPI_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
2. Place R1 closer to driver side to effectively damping the undershoot and overshoot.
3. All TPM branches/connections (TPM_MOSI, TPM_MISO, TPM_CLK, and PCH_CS2#) can be left as I/O if SPI TPM is not implemented.



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Title			
Flash(KBC+PCH)/RTC			
Size A3	Document Number		Rev
	Brook BH		-1M
Date:	Wednesday, February 04, 2015		Sheet 25 of 106



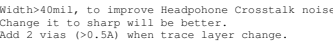
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Title Thermal 7718/Fan Controller P2793		
Size A3	Document Number Brook BH	Rev -1M
Date: Wednesday, February 04, 2015	Sheet 26 of 106	

SSID = AUDIO



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Audio Codec ALC255

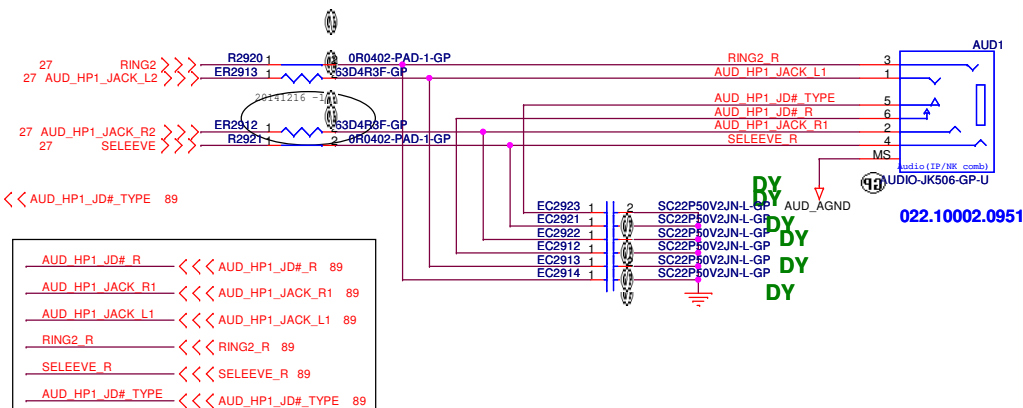
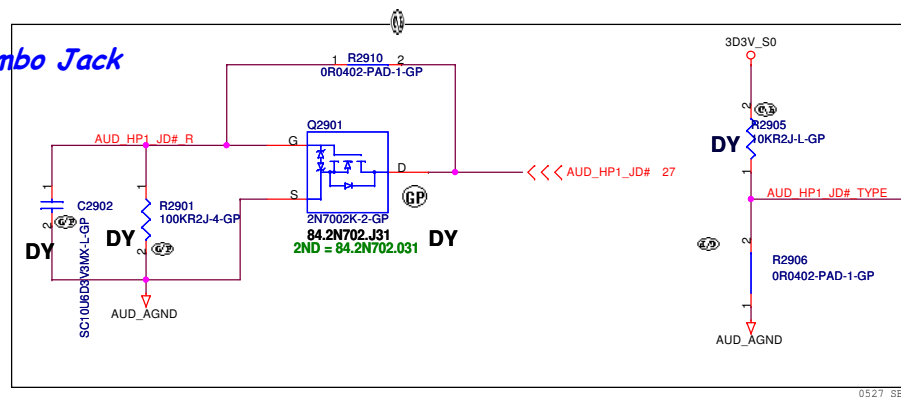
A2	Brook BH
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Date: Wednesday, February 04, 2015 Sheet 27 of

Speaker



Trace width=40mil



AFTP TESTPOINT

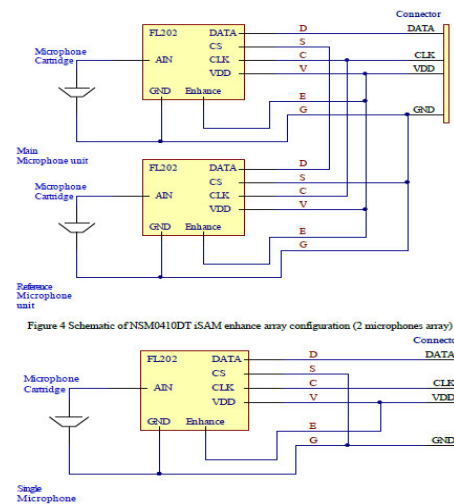
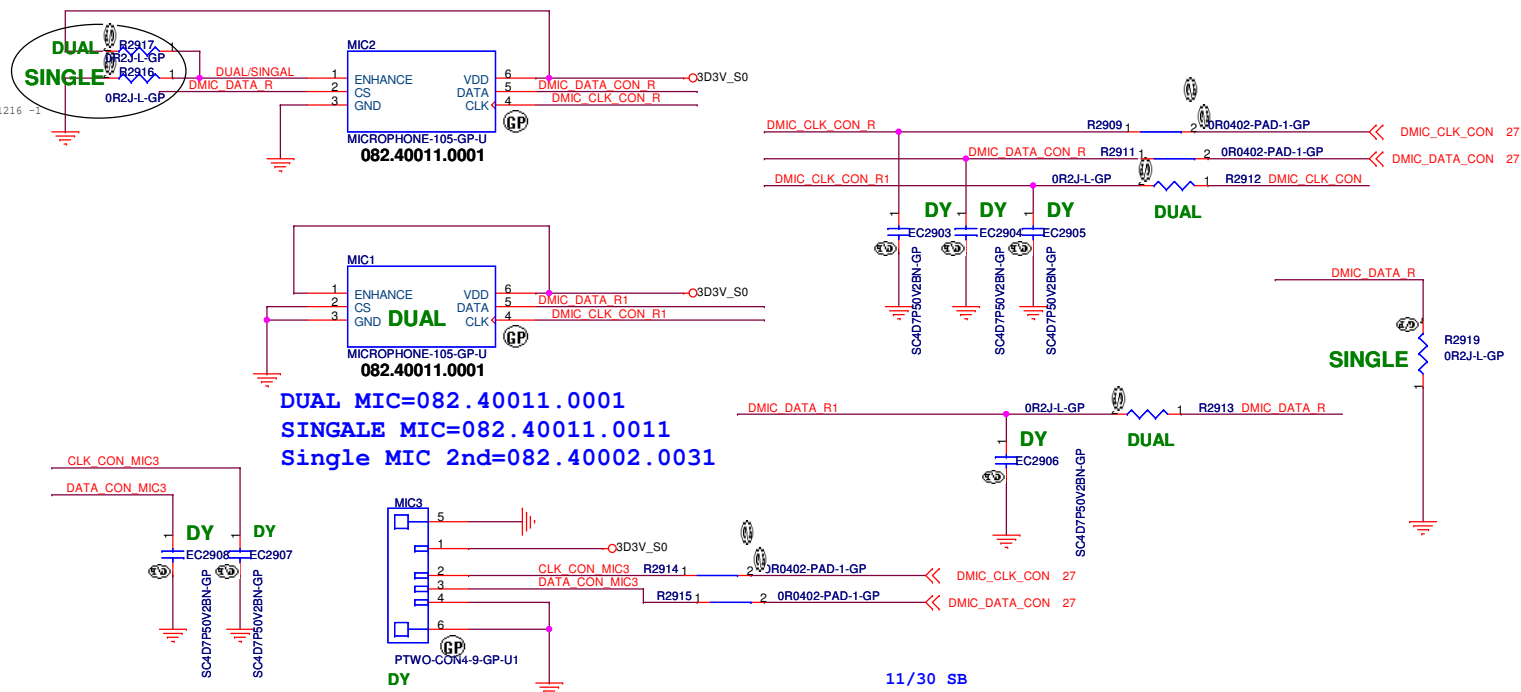


Figure 4 Schematic of NSM0410DT iSAM enhance array configuration (2 microphones array)

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Audio Jack

Size

Document Number

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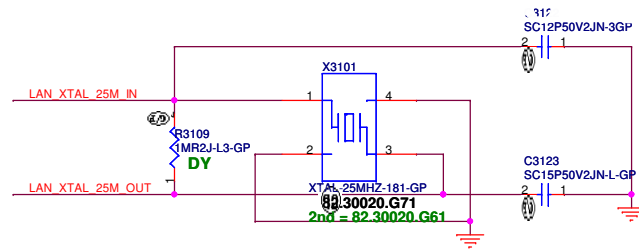
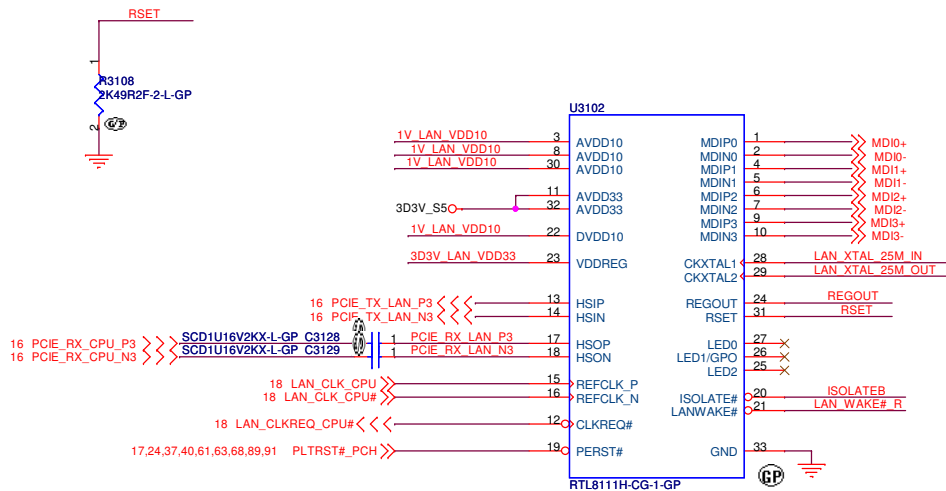
Rev

Date _____

Thursday, February 12, 2015

Sheet 29 of 106

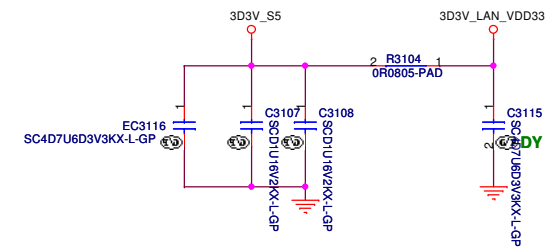
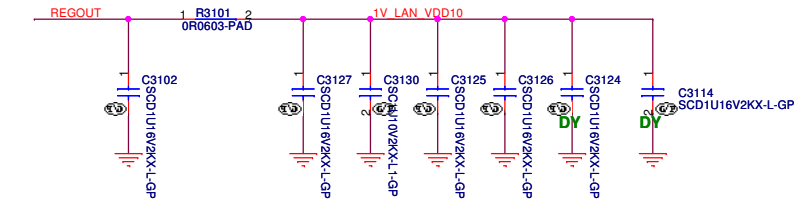
106



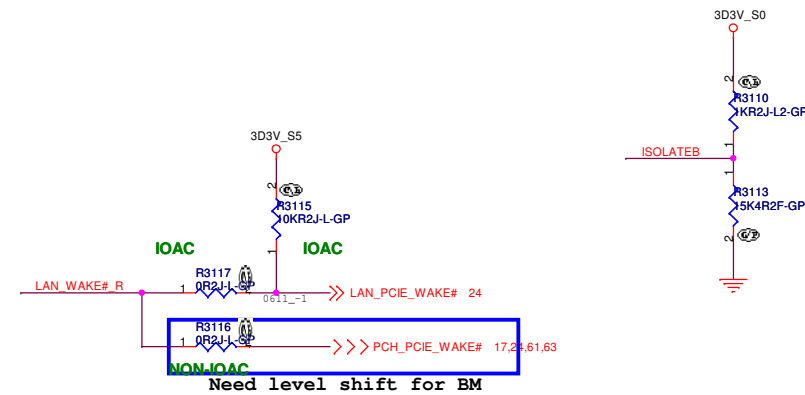
For RTL8111G(S)

* Place C3121 to C3124 close to each VDD10 pin-3, 8,

C3124: close to Pin8
C3125: close to Pin30
C3126: close to Pin3
C3127: close to Pin22



C3108: close to Pin32
C3107: close to Pin11 (RTL8111 only)



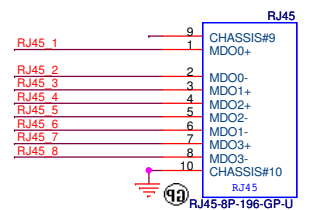
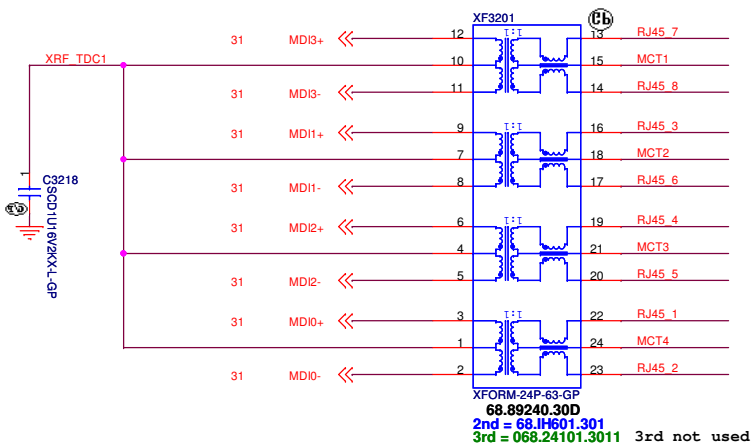
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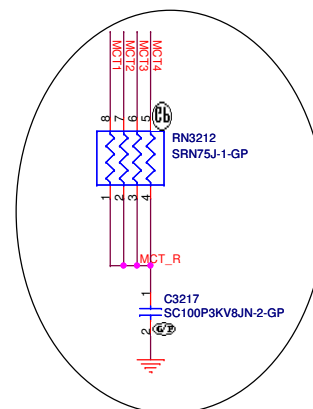
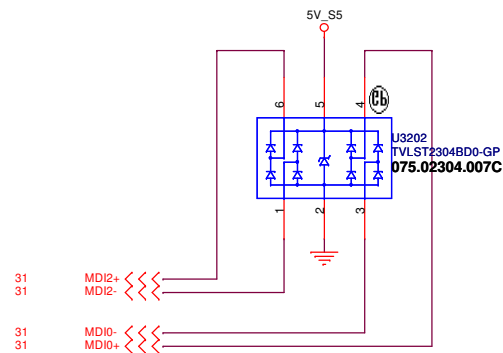
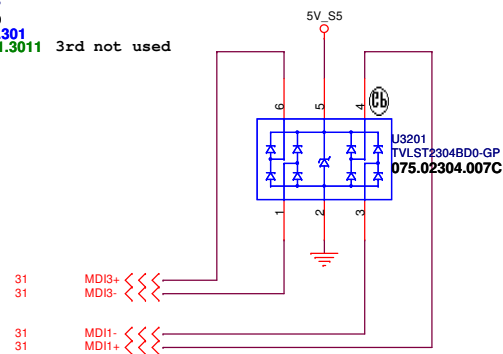
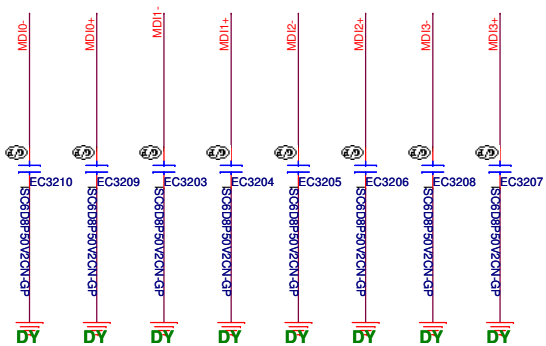
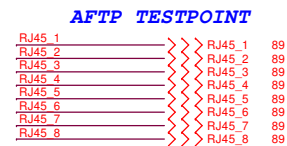
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Title		
LAN (RTL8111G(S))		
Size A3	Document Number	Rev
	Brook BH	-1M
Date: Wednesday, February 04, 2015	Sheet 31	of 106

SSID = LAN



022.10001.00F1
2nd = 022.10001.0F21



12/23 修改家電下鄉 PD

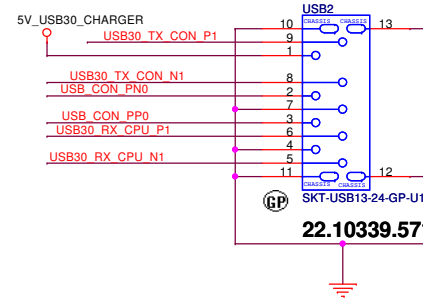
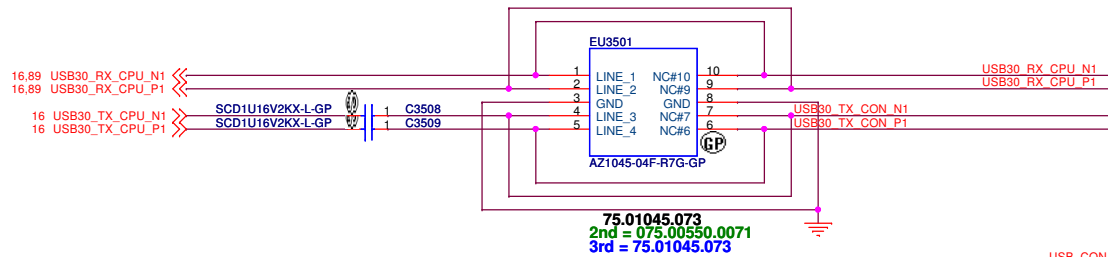
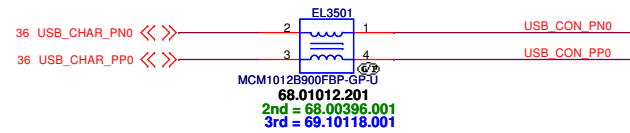
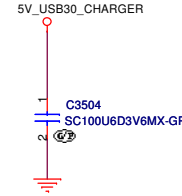
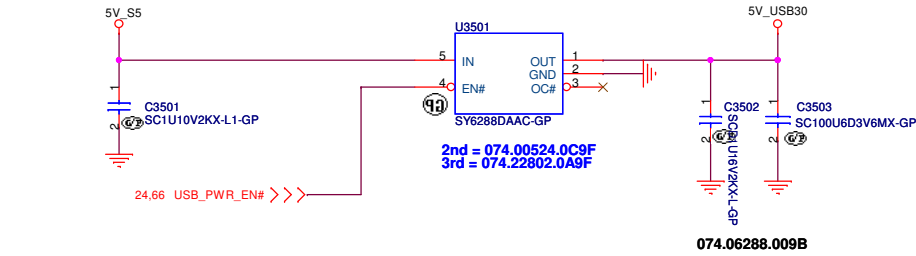
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Title			
(LAN+VGA) CONNECTOR			
Size A3	Document Number		Rev
	Brook BH		-1M
Date:	Wednesday, February 04, 2015	Sheet 32 of	106

Low Active 2A

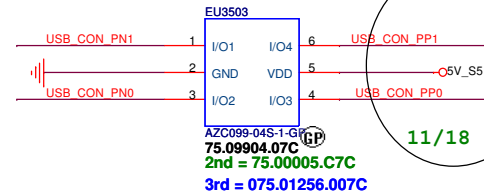


USB 3.0 Connector Pin definition

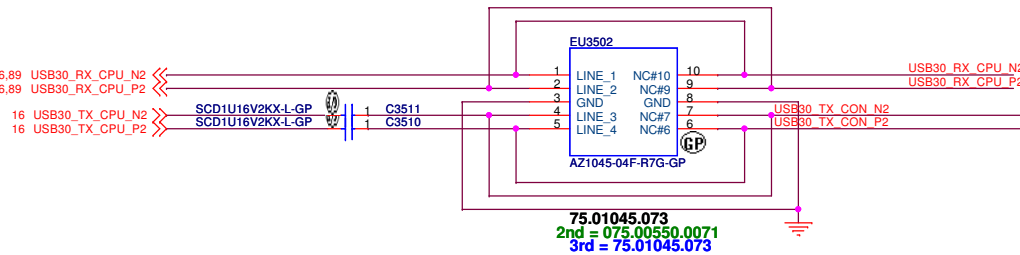
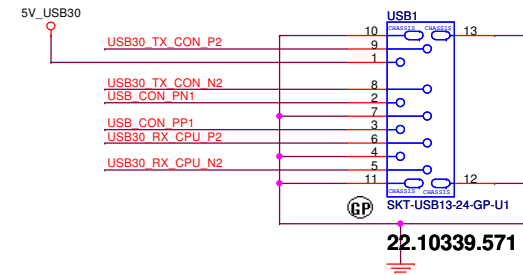
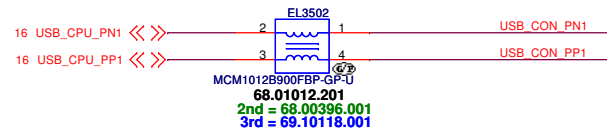
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

AFTP TESTPOINT

USB30_TX_CON_P1	USB30_TX_CON_P1	89
USB30_TX_CON_N1	USB30_TX_CON_N1	89
USB_CON_PN0	USB_CON_PN0	89
USB_CON_PP0	USB_CON_PP0	89
USB30_RX_CPU_P1	USB30_RX_CPU_P1	16,89
USB30_RX_CPU_N1	USB30_RX_CPU_N1	16,89
USB30_TX_CON_P2	USB30_TX_CON_P2	89
USB30_TX_CON_N2	USB30_TX_CON_N2	89
USB_CON_PN1	USB_CON_PN1	89
USB_CON_PP1	USB_CON_PP1	89
USB30_RX_CPU_P2	USB30_RX_CPU_P2	16,89
USB30_RX_CPU_N2	USB30_RX_CPU_N2	16,89



11/18 SB Change to 5V_S5

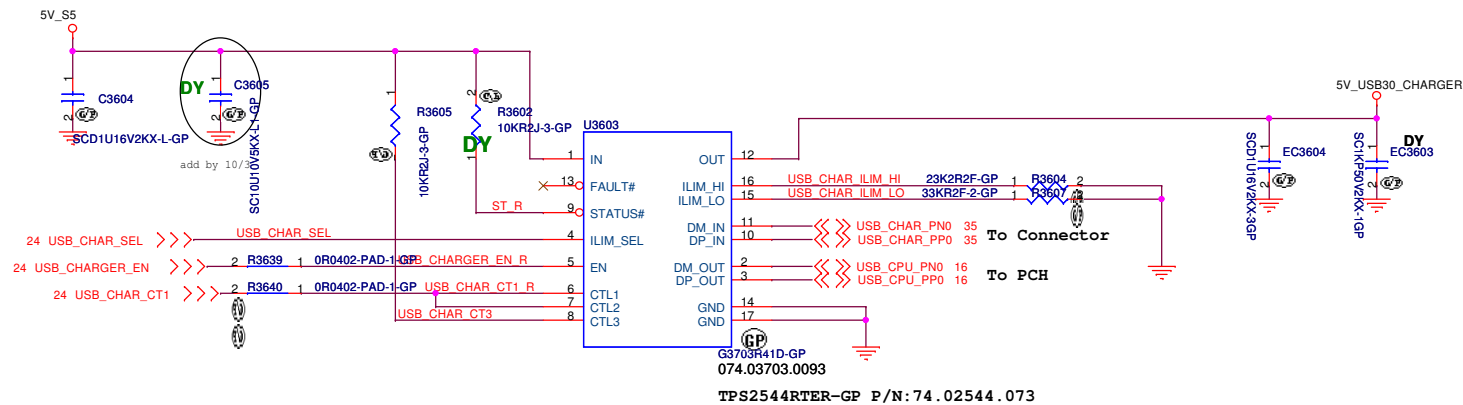


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Title	USB 3.0	Rev	-1M
Size	Document Number	Brook BH	
Date	Tuesday, February 10, 2015	Sheet	35 of 106



20150115 -1

Device Control Pins				
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	0
DCP_Auto	0	1	1	X

3.Electrical Safety for USB3.0 Port

2.0 A \leq Measurement value \leq 2.2 A : Pass

1.9 A \leq Measurement value $<$ 2.0 A or 2.2 A $<$ Measurement value \leq 2.4 A : Marginal

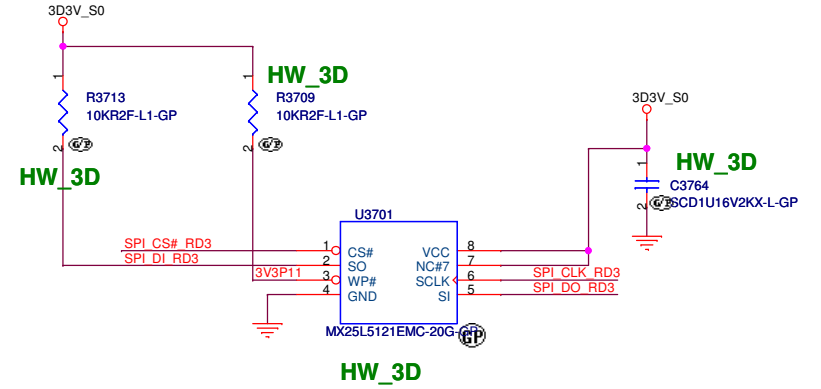
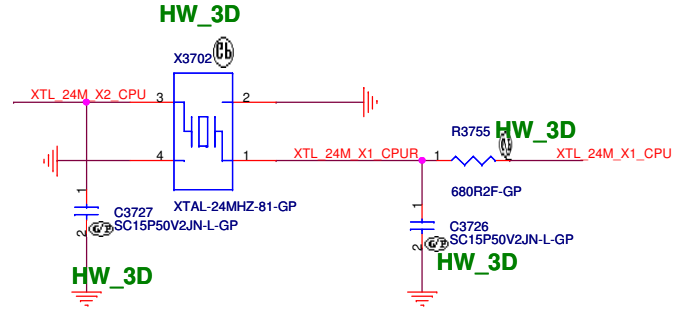
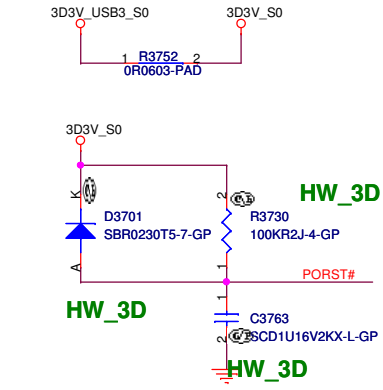
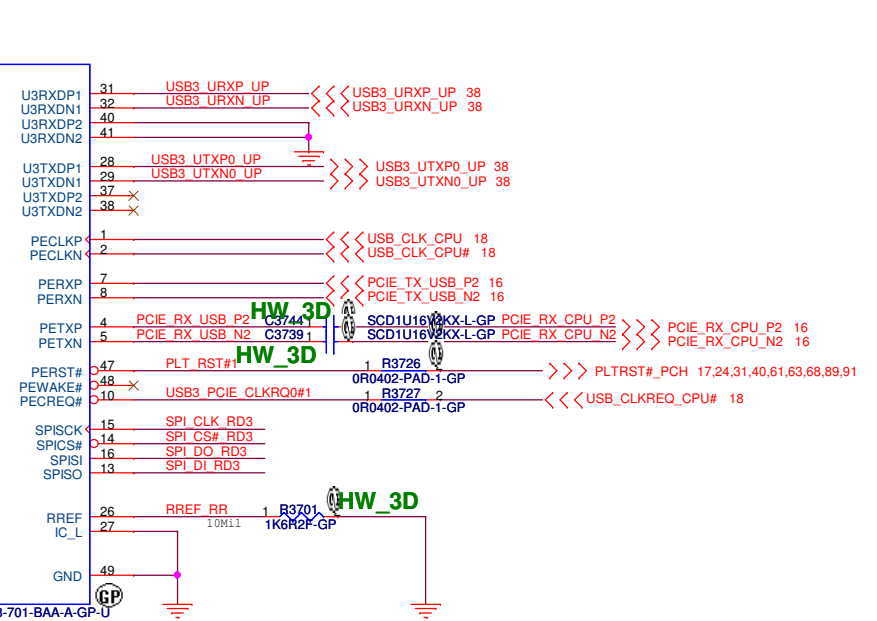
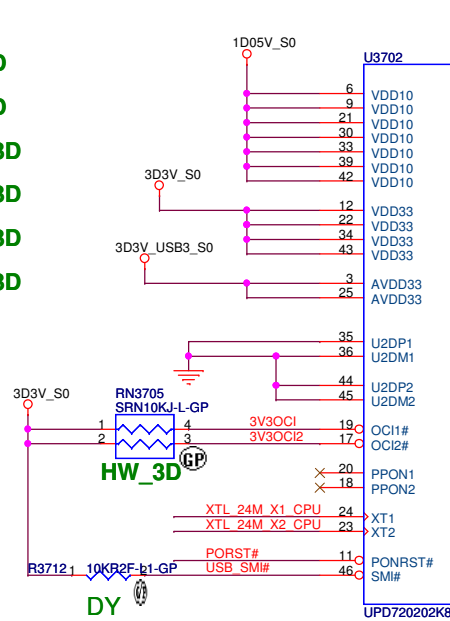
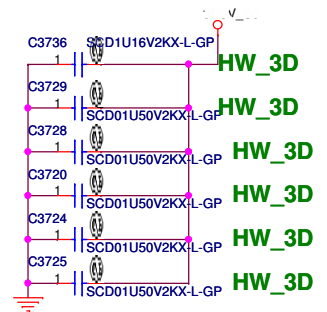
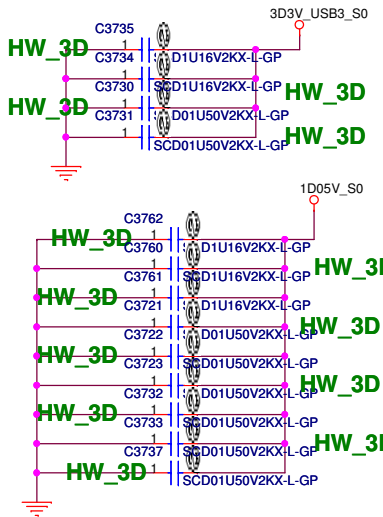
If this result is "Marginal", 4 more samples (Total 5 samples) must be measured for each port.

And it must be confirmed that the values of 5 samples can meet our requirement (1.9 A - 2.4 A).

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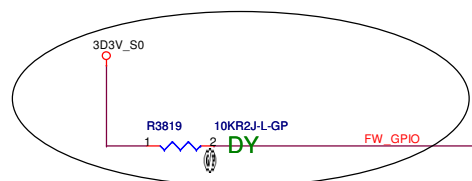
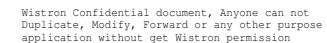
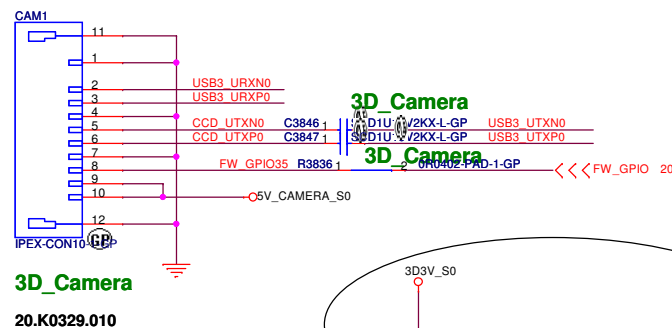
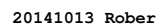
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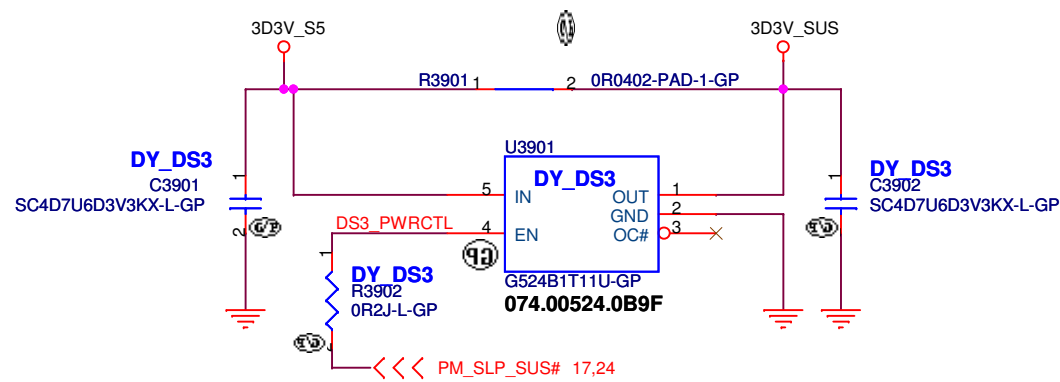
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Title USB Charger			
Size A3	Document Number		Rev -1M
Date: Wednesday, February 04, 2015		Sheet 36 of 106	Brook BH



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Title PCIE to USB		
Size B	Document Number Brook BH	Rev -1M
Date: Wednesday, February 04, 2015	Sheet 37	of 106





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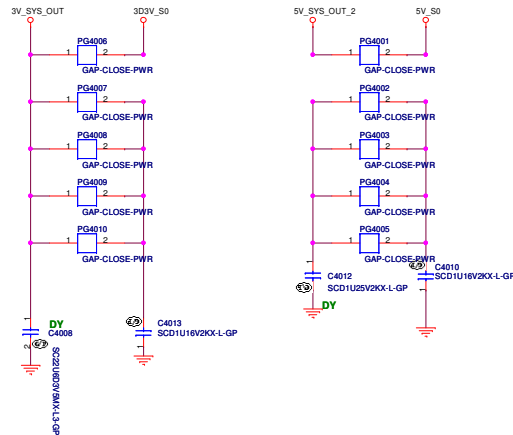
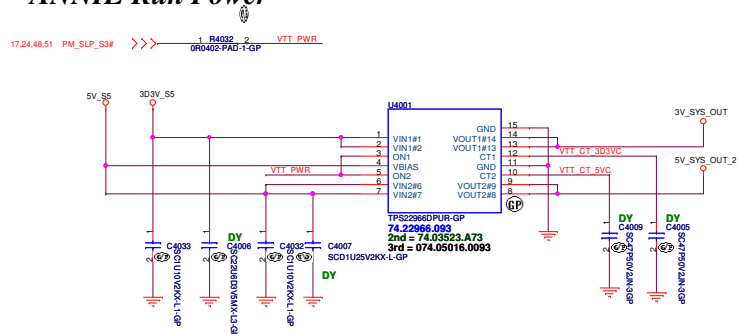
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Title			
DS3			
Size A4	Document Number		Rev
	Brook BH		-1M
Date:	Wednesday, February 04, 2015	Sheet 39	of 106

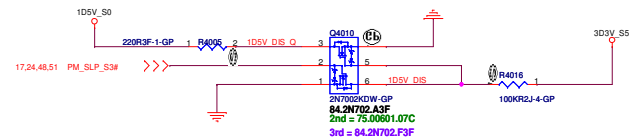
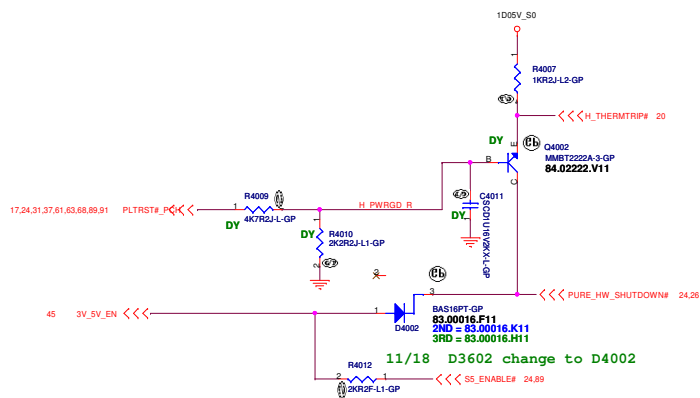
Power Sequence



ANNIE Run Power



Discharge circuit



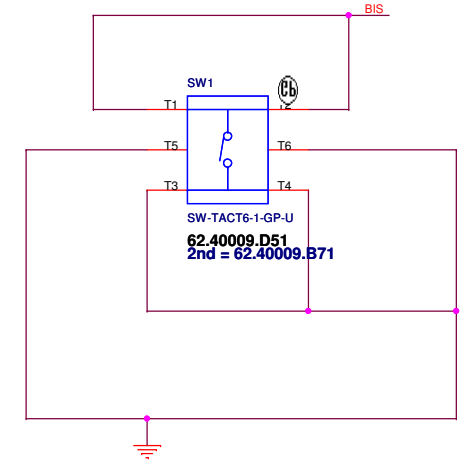
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Title		
Connected Standby1		
Size A2	Document Number	Rev
	Brook BH	-1M
Date:	Wednesday, February 04, 2015	Sheet 40 of 106

Battery Insert

[illegible]

SSID = PWR.Plane.Regulator_3p3v5v

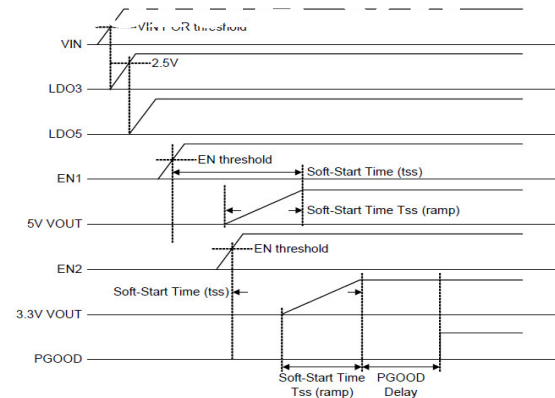
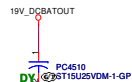
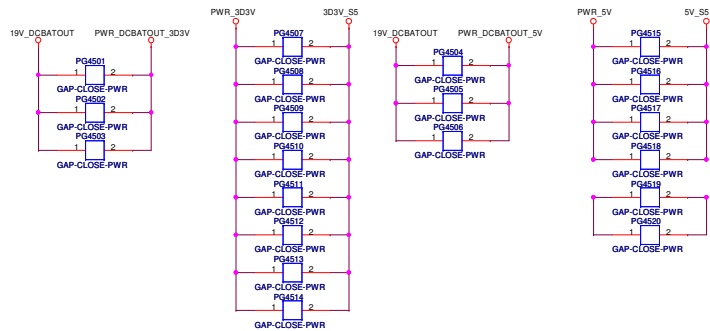
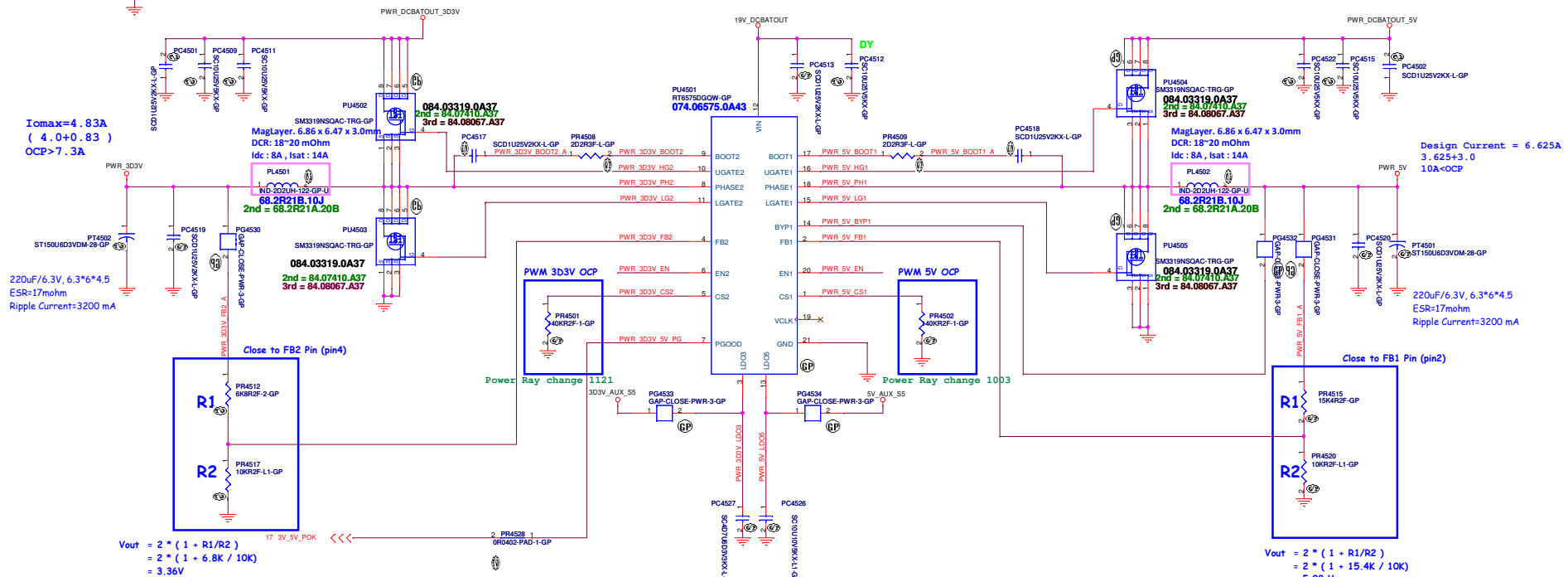
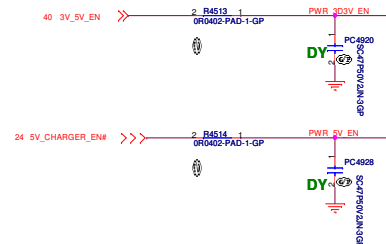


Figure 6. RT6575B Timing

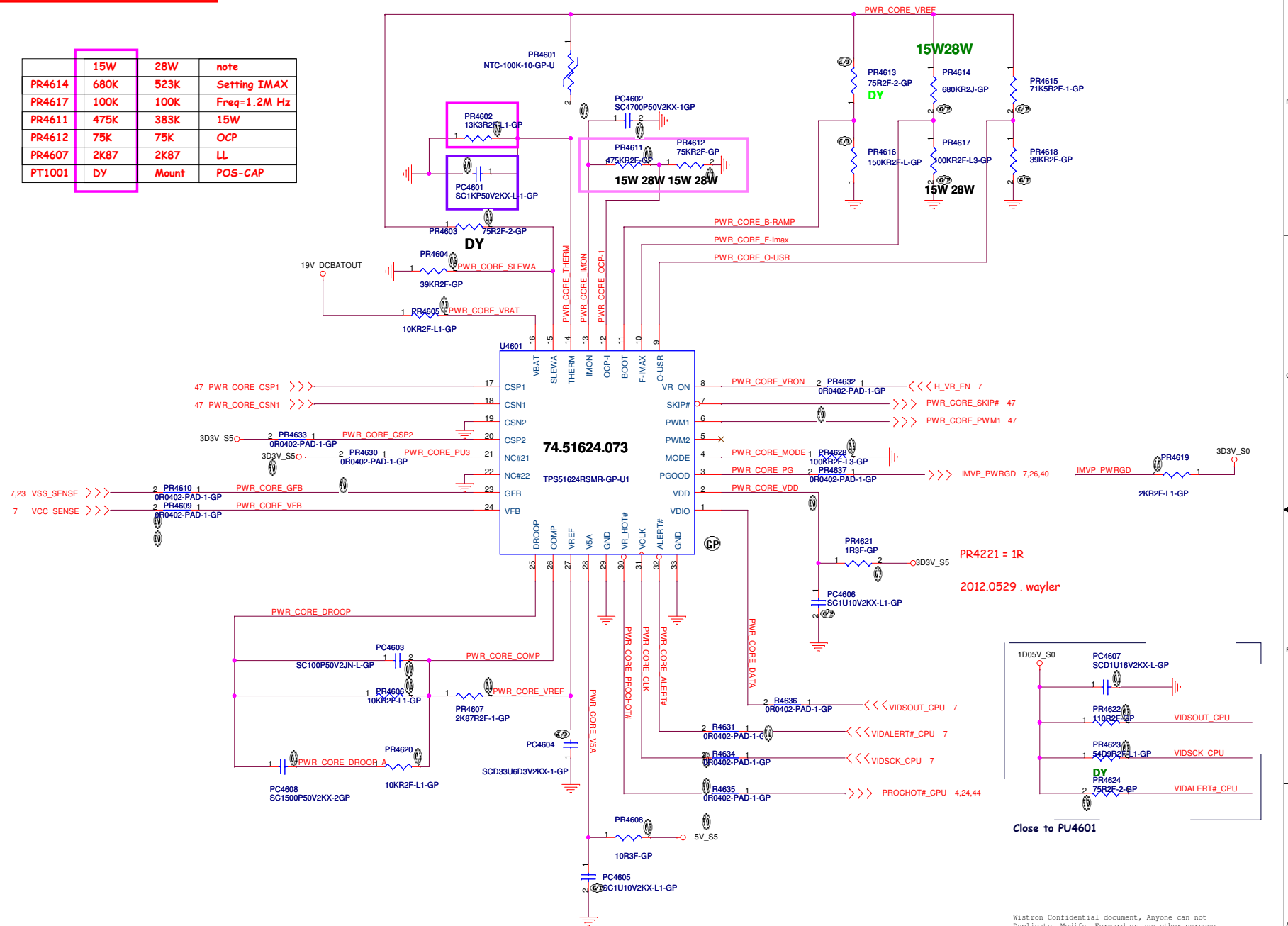


11/18 R4913 and R4914 need to change R4513and R4514



SSID = CPU.Regulator

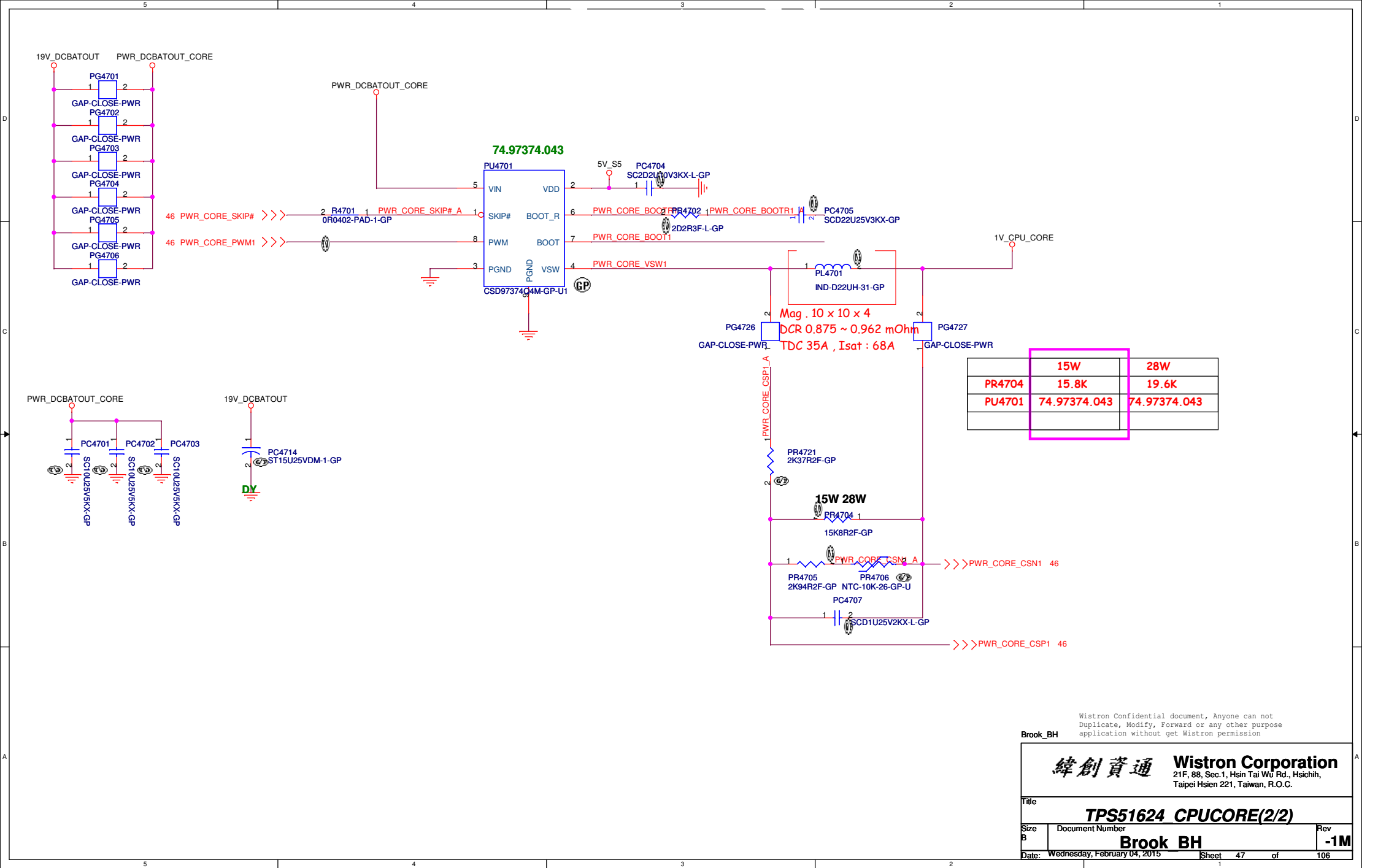
	15W	28W	note
PR4614	680K	523K	Setting IMAX
PR4617	100K	100K	Freq=1.2M Hz
PR4611	475K	383K	15W
PR4612	75K	75K	OCF
PR4607	2K87	2K87	LL
PT1001	DY	Mount	POS-CAP

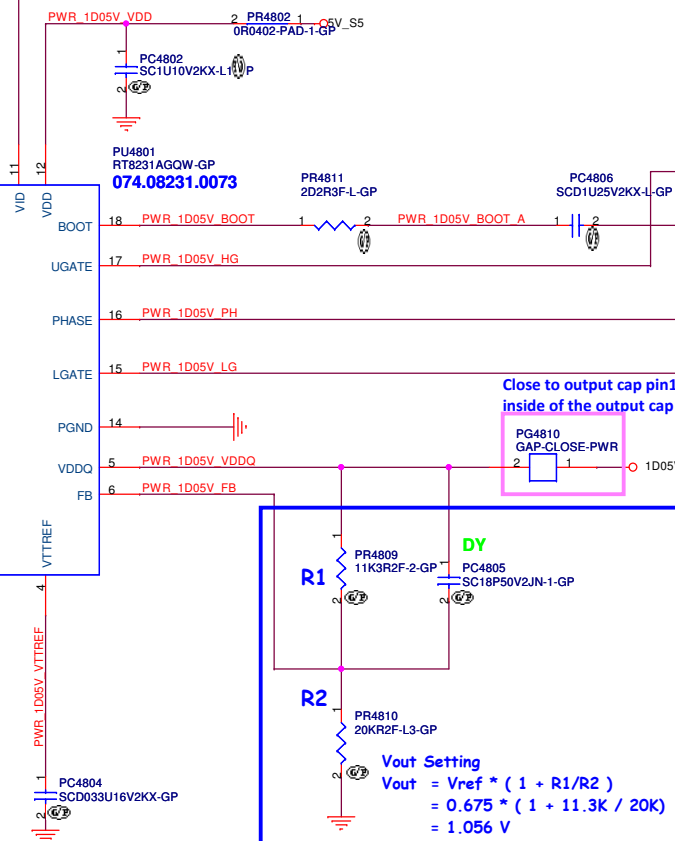
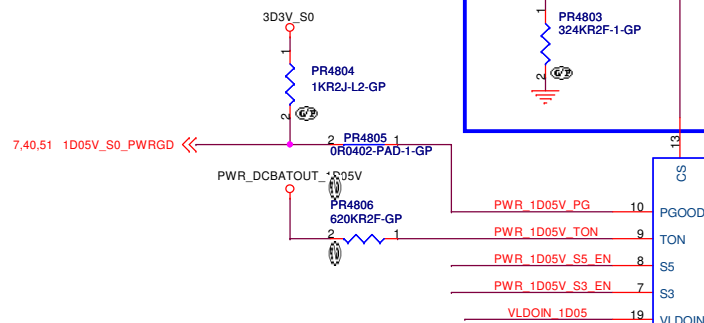
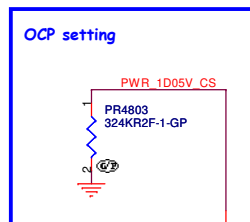
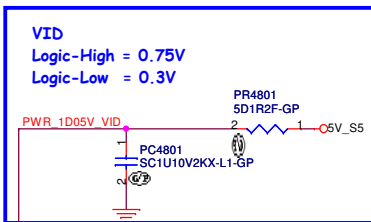
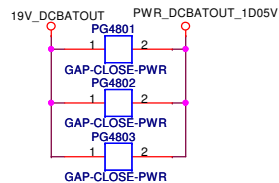


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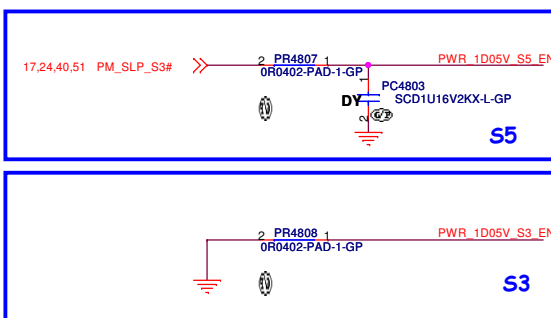
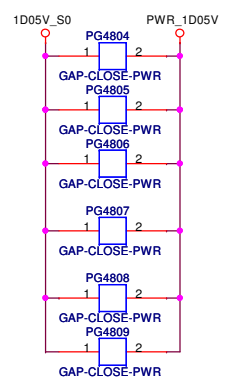
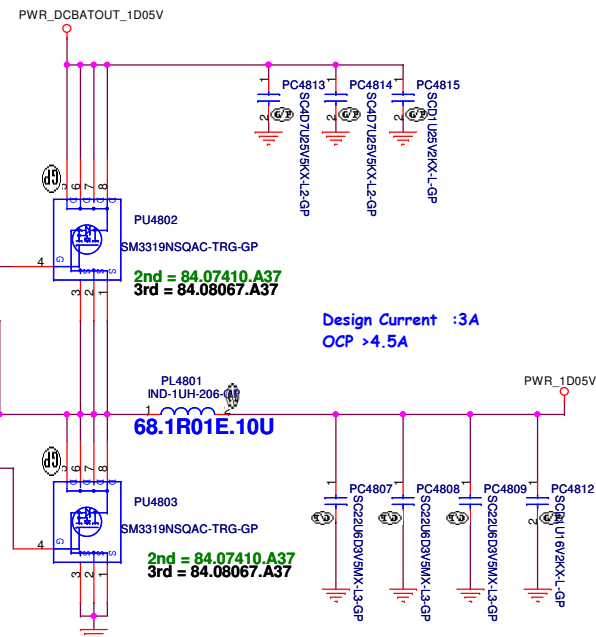
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Title			
TPS51624 CPUCORE(1/2)			
Size	Document Number		Rev
Custom	Brook_BH		-1M
Date:	Wednesday, February 04, 2015	Sheet 46 of	106





VID vs Vref Table
 VID Logic-High => Vref = 0.675 V
 VID Logic-Low => Vref = 0.75 V
 note. Vref can only be changed from 0.675v to 0.75v after power-on



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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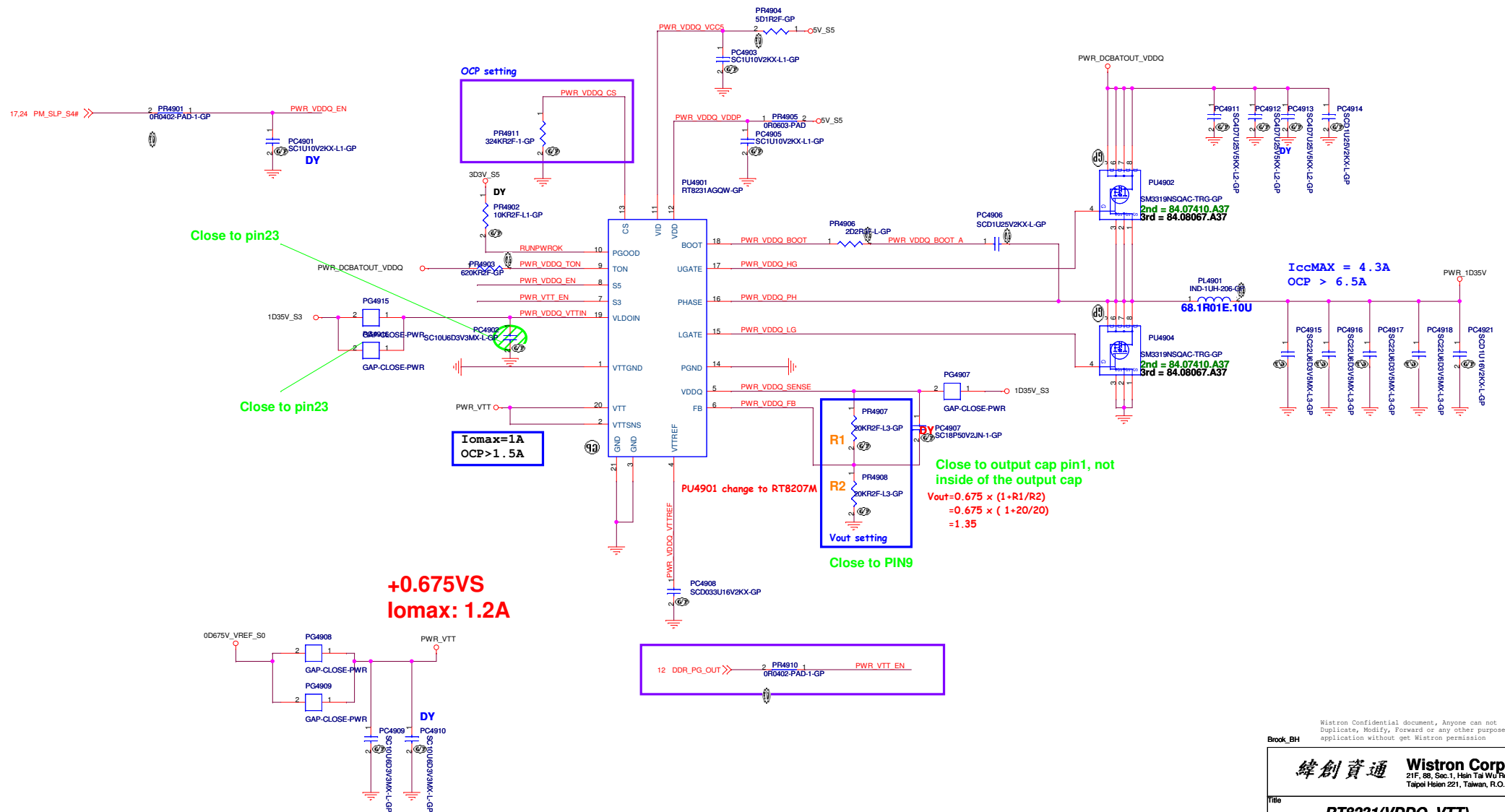
Title: **DC to DC 1D05V(SY8208D)**

Size A3 Document Number **Brook BH** Rev **-1M**

Date: Thursday, February 05, 2015 Sheet 48 of 106

```
SSID = PWR.Plane.Regulator_1p2v0p6v
```

RT8231 for VDDQ



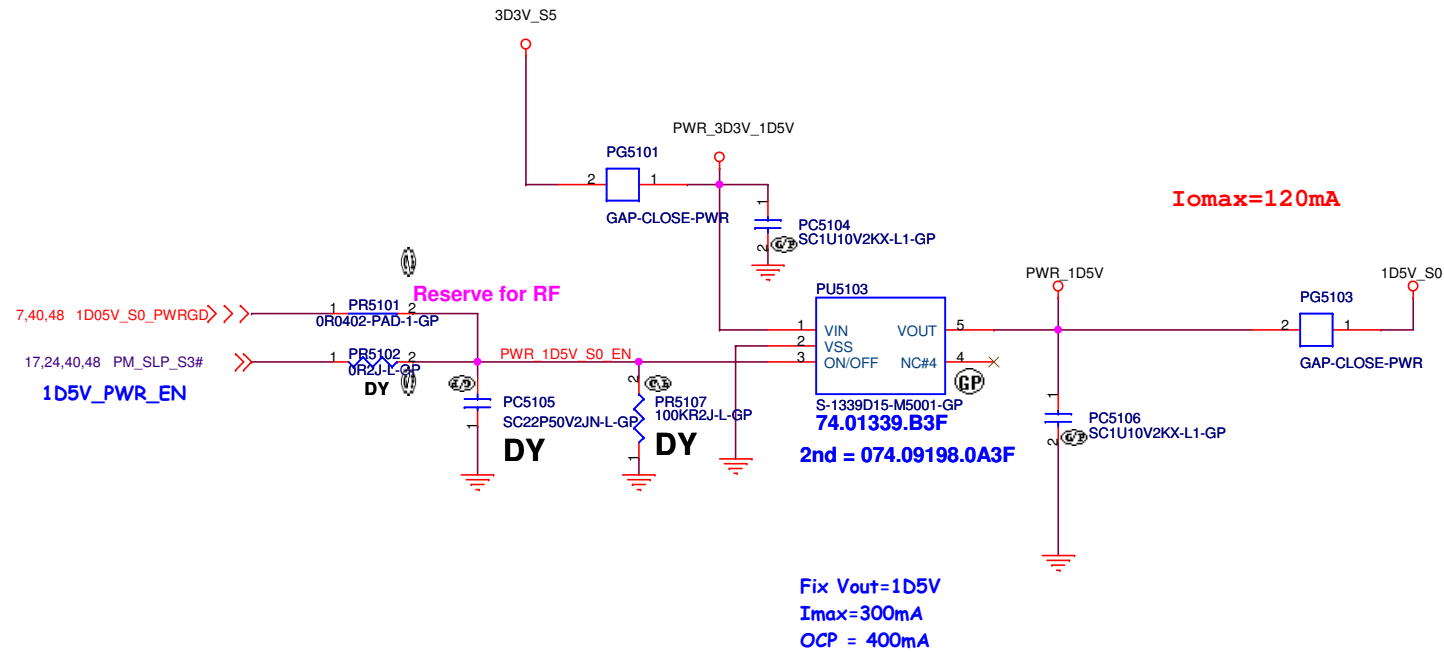
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RT8231(VDDQ_VTT)			
Size	Document Number	Rev	
Custom	Brook BH	-1M	
Date:	Wednesday, February 04, 2015	Sheet 49 of	106

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



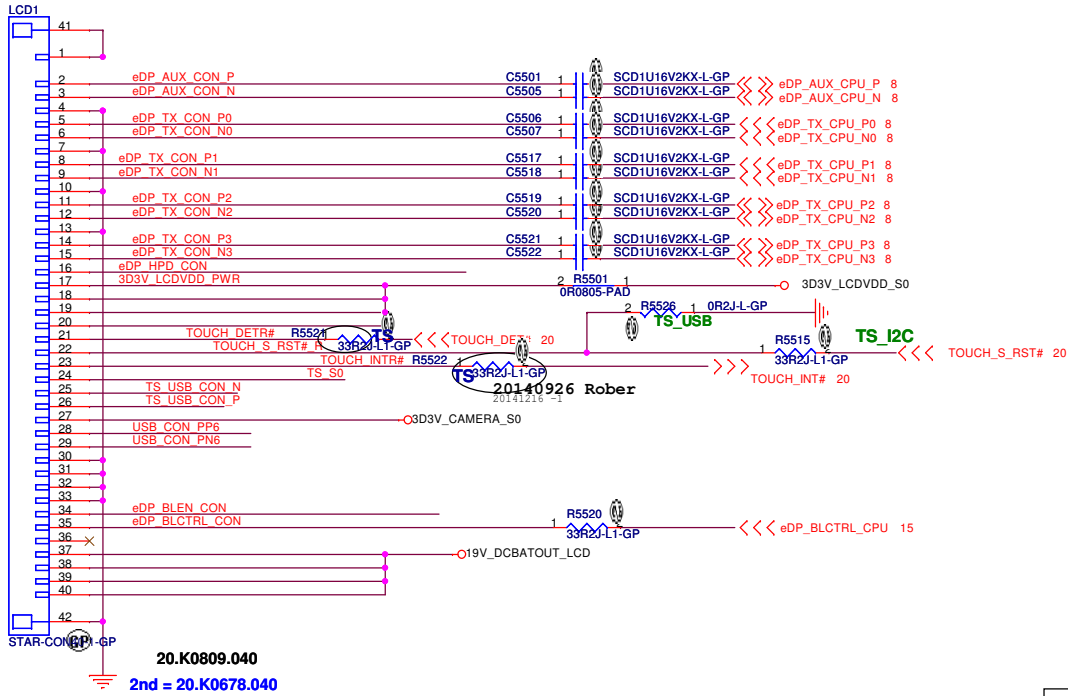
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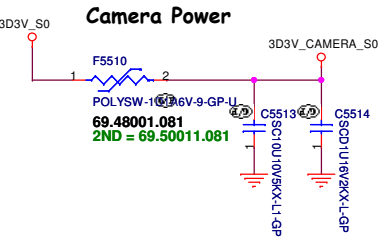
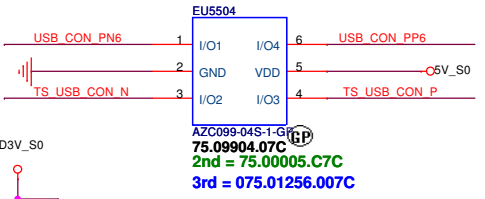
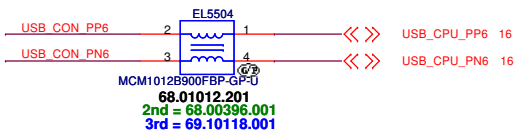
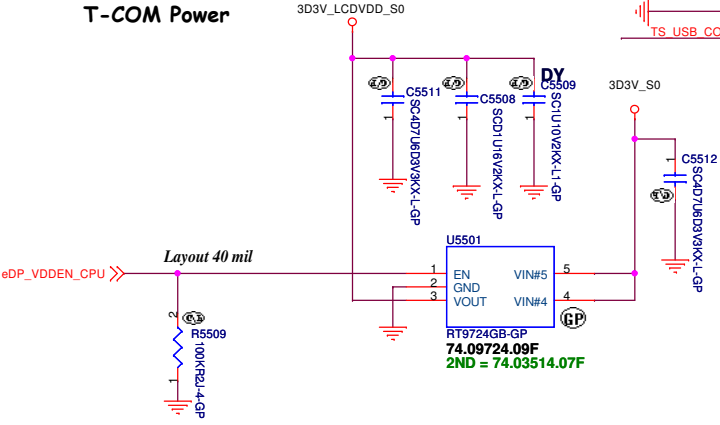
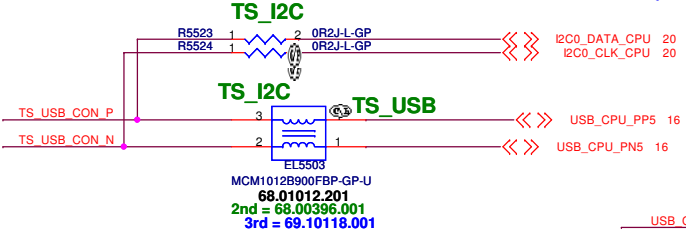
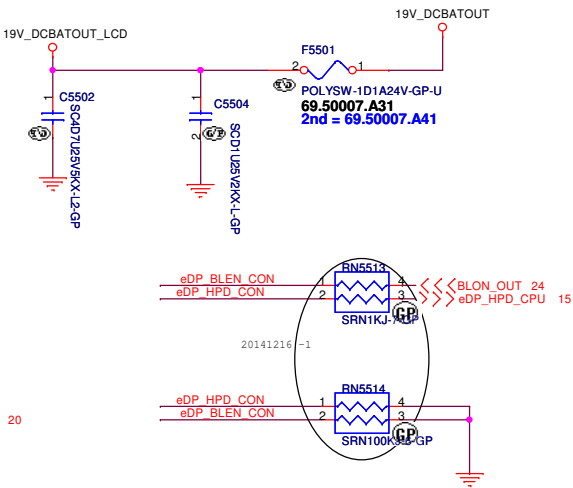
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Title			
1D5V_S0 SYW232			
Size Custom	Document Number		Rev
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Date:	Wednesday, February 04, 2015	Sheet 51 of	106

Main Func = LCD

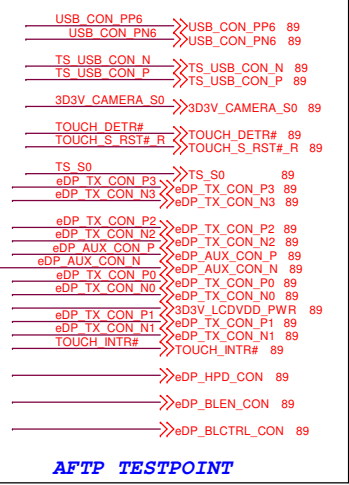
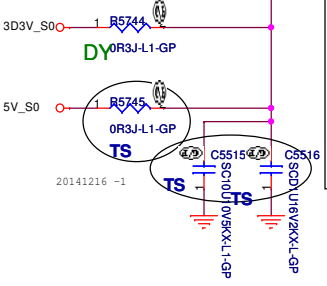
Pin count		EDP 4Lans+CCD
1		GND
2		eDP_AUX_CON_P
3		eDP_AUX_CON_N
4		GND
5		eDP_TX_CON_P0
6		eDP_TX_CON_N0
7		GND
8		eDP_TX_CON_P1
9		eDP_TX_CON_N1
10		GND
11		eDP_TX_CON_P2
12		eDP_TX_CON_N2
13		GND
14		eDP_TX_CON_P3
15		eDP_TX_CON_N3
16		eDP_HPD_CON
17		LCDVDD(3V)
18		LCDVDD(3V)
19		LCDVDD(3V)
20		LCDVDD(3V)
21		TOUCH_DETR#
22		TOUCH_GND/ TOUCH_RST
23		TOUCH_EN/ TOUCH_INT
24		Touch_PWR(3V/5V)
25		USB_PN6/ SCL
26		USB_PP6/ SDA
27		3D3V_CAMERA_S0
28		USB_CAMERA_P
29		USB_CAMERA_N
30		GND
31		GND
32		GND
33		GND
34		GND
35		
36		
37		DCBATOUT_LCD
38		DCBATOUT_LCD
39		DCBATOUT_LCD
40		DCBATOUT_LCD



Inverter Power



Touch panel Power



<Core Design>

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Title LCD Connector

Size A3 Document Number Brook BH Rev -1M

Date: Thursday, February 12, 2015 Sheet 55 of 106

SSID = Display

VGA RTD2168

Embedded LDO
Select VCCK_V12 source from external 1.2V or embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

close to pin25

close to pin24

close to pin5

close to pin9

close to pin20

those compoent need to close

L5601~3 change to 68.00084.B61

20140926 Rober

20141013 Rober

close to pin19

AFTP TESTPOINT

D-SUB-15-155-GP-U

20.20984.015

2nd = 20.20938.015

Mode Configure Table(Power On Latch)

	POL1_SDA(PIN22)	
	0	1
POL2_SCL(PIN23)	0	X
	1	ROM ONLY MODE
		EEPROM MODE

RTD2168 Supports three operation mode for systemdesign.
Reserve 4.7K resistor pull high/low for mode selection
ROM ONLY Mode: PIN22 pull low, PIN23 pull high
EP Mode: PIN22 pull high, PIN23 pull low
EEPROM Mode: PIN22 pull high, PIN23 pull high

EEPROM MODE

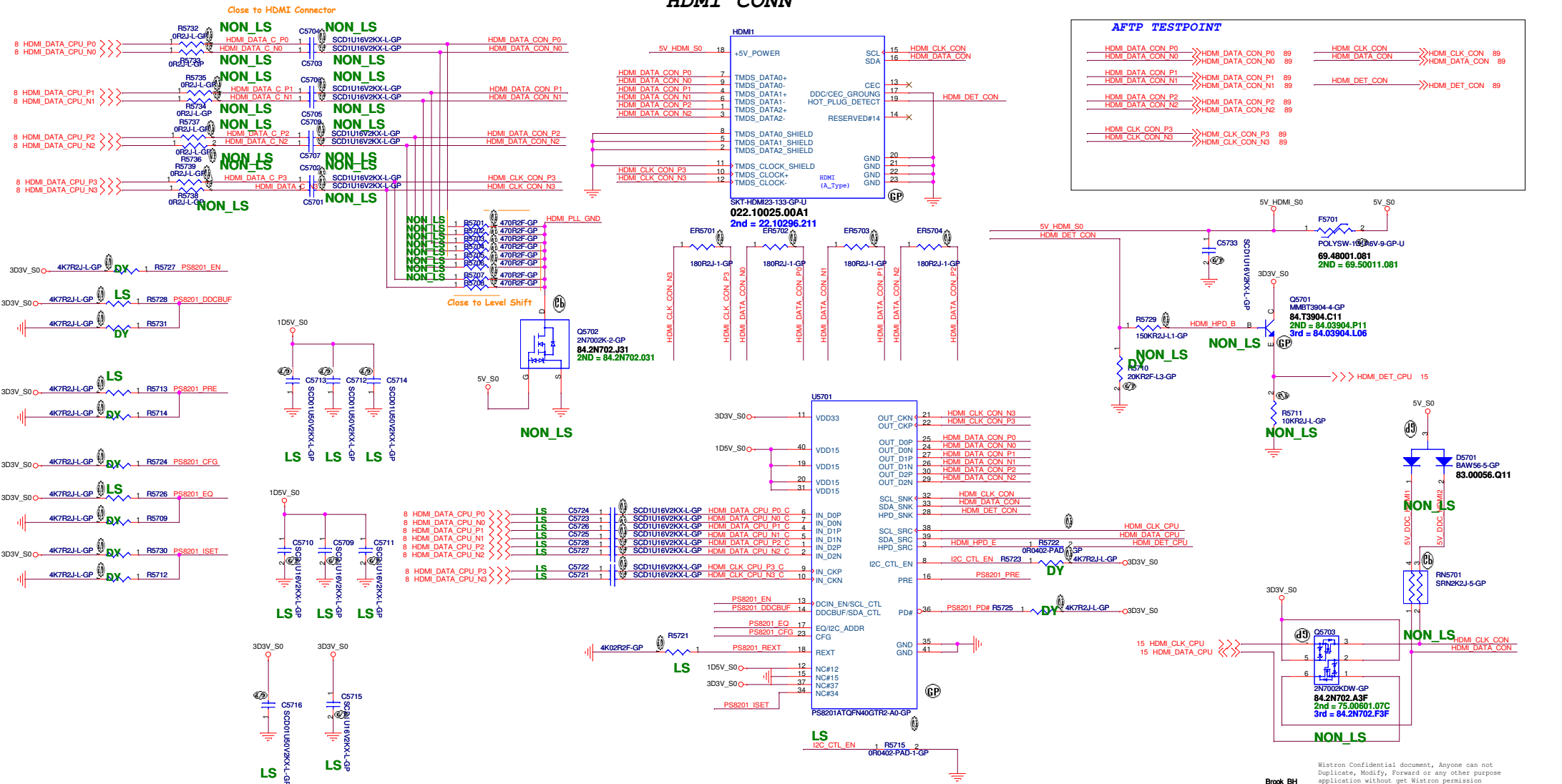
VEDOR CHECK

In EEPROM mode, an additional EEPROM is needed. EEPROM should configure with following conditions.
1- EEPROM with a size of 16K-Byte
ROM or EEPROM mode: connect to PCH SMBUS
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA6

HDMI Level Shifter & CANN

HDMI CONN

AFTP TESTPOINT



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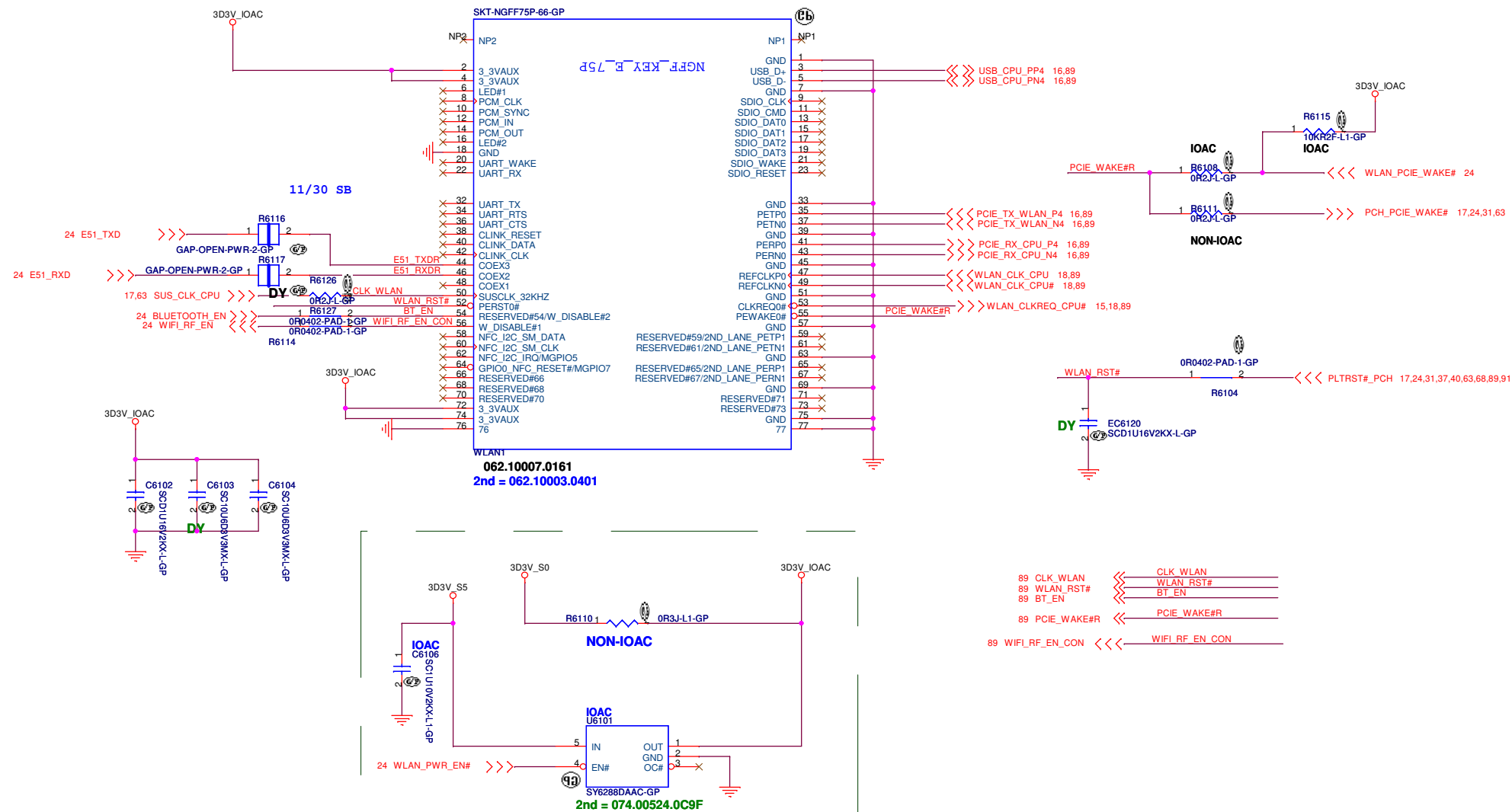
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HDMI Level Shifter&Conn

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Title

Mini Card WLAN

Size

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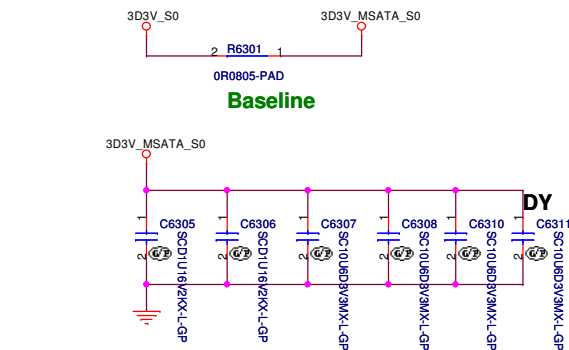
Date: Wednesday, February 11, 2015

Sheet 6

106

SSID = mSATA

Mini Card Connector(mSATA)



Baseline Baseline Baseline BaselineBaseline

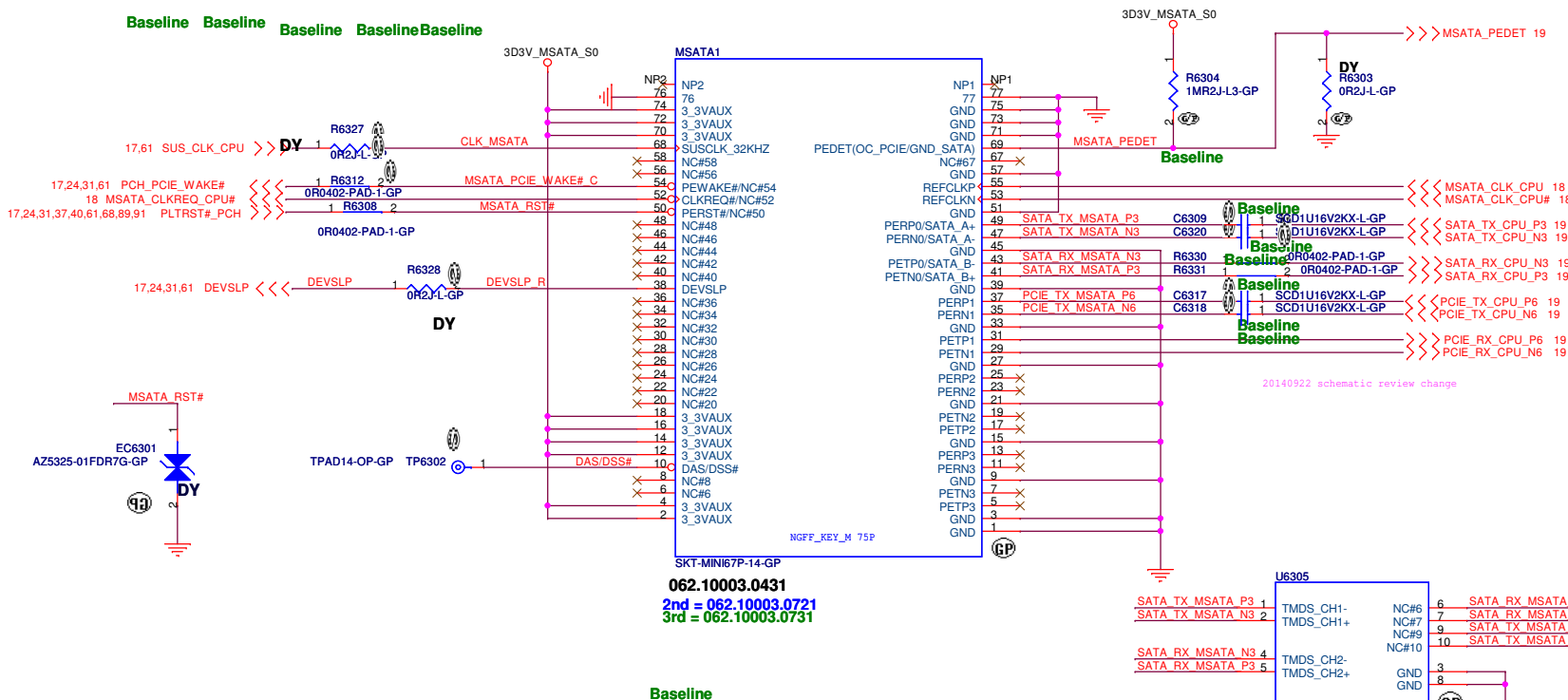


Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface ¹	Port Configuration ²
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

17.2.6 General Guidelines for mSATA (Gen 2 and Gen 3) Routing on SATA/PCIe muxed Ports

The below table summarizes the AC cap requirements on the motherboard when using the SATA/PCIe muxed ports.

Table 17-6. SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF ²	None ³

Notes:

1. For PCIe only application, please refer to the PCIe guidelines for details.
2. For SATA only application, both PCH Tx and PCH Rx channels need to have 10 nF caps on the motherboard. This option supports all SATA devices. However, the PCH Rx 10 nF capacitor can be removed if DC coupled ODDs/devices are NOT used.
3. For PCIe/SATA mixed application, a 100 nF AC cap is required on motherboards for PCH Tx channel and NO AC cap is required on motherboard for the PCH Rx channel. This option DOES NOT support DC coupled ODDs/Devices.

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

- ** Native: Internal Pull-Up (15k-40k) when function.**

2/5 PD Rober Part number change with EU3501

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

- ** Native: Internal Pull-Up (15k-40k) when function.

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Title

MSATA Conn

Size

Document Number

Brook BH

Date _____

Thursday, February 12, 2015

10

Sheet

63

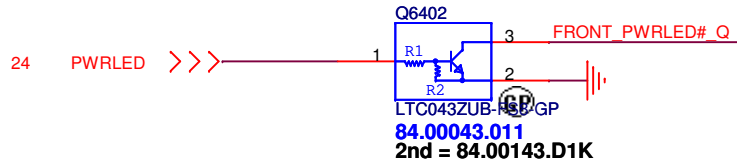
9

106

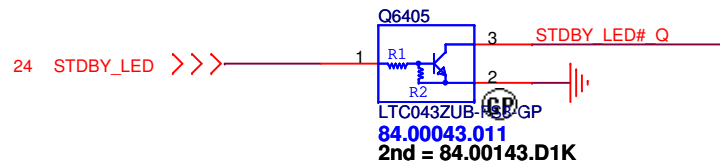
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SSID = User.Interface

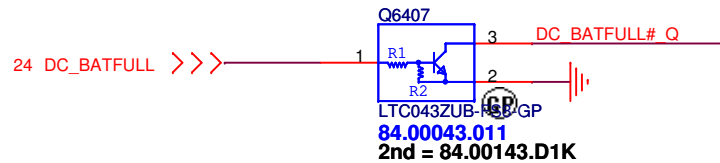
Power Button_LED



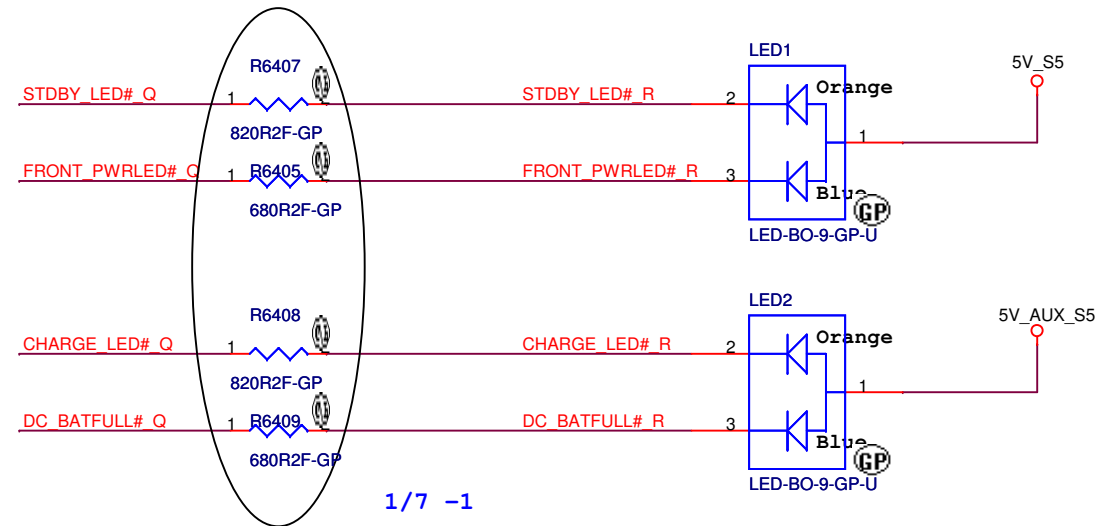
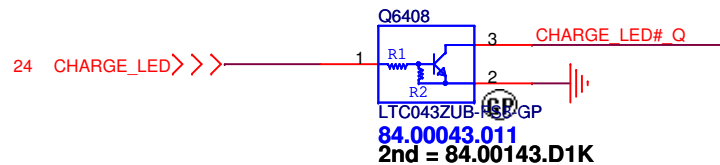
Power STDBY_LED



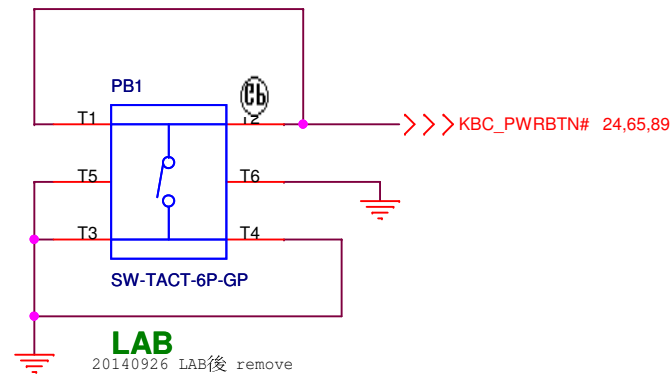
Battery LED2 (DC_BATFULL)



Battery LED1 (CHARGE)



Power Button



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Title

LED Bard/Power Button

Size
A4

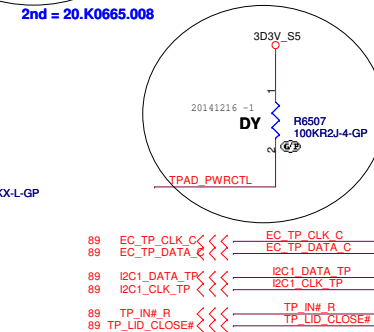
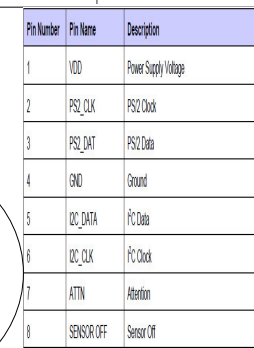
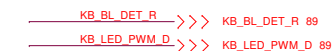
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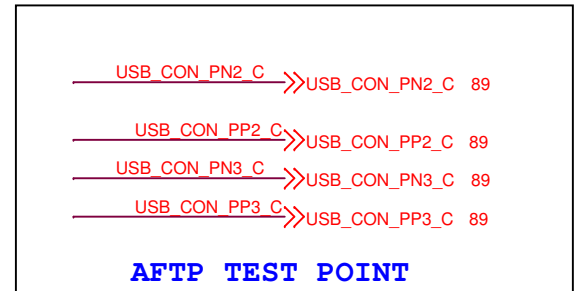
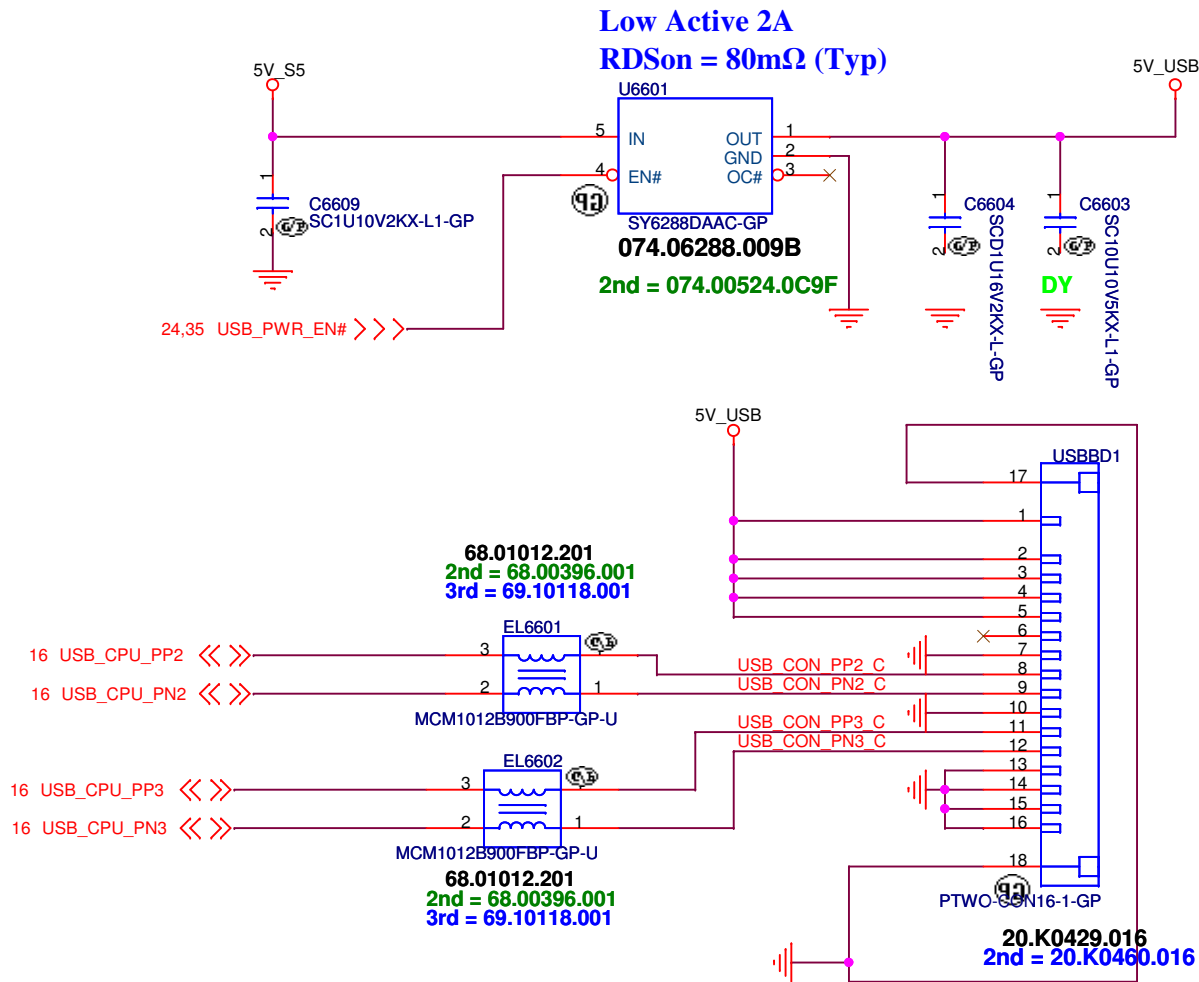
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Sheet 64 of 106

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<p>Key Board/Touch Pad</p>		<p>Rev</p>	
<p>Size Custom</p>	<p>Document Number</p>		<p>-1M</p>
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20150112 Rober

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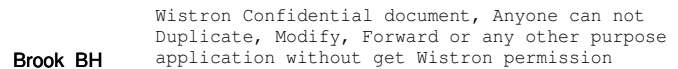
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Date: Wednesday, February 04, 2015

Sheet 66 of 106



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Hall Sensor

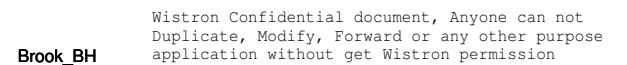
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Rev	-1M
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Date: Wednesday, February 04, 2015

Sheet 67 of 106



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Dubug connector

Brook BH

-1 M

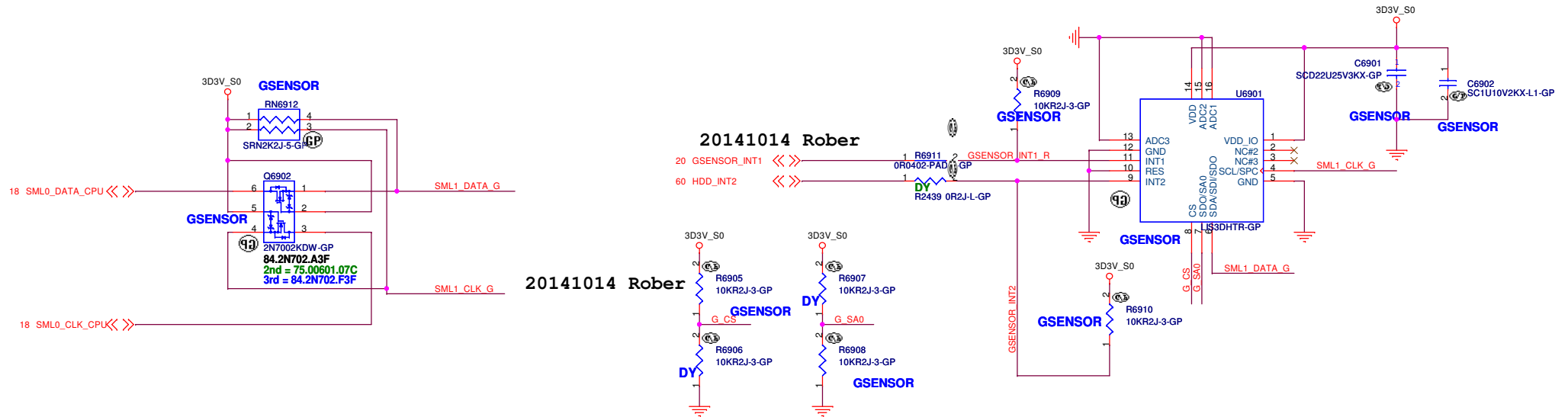
Sheet 68 of 106

SSID = User.Interface

G Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

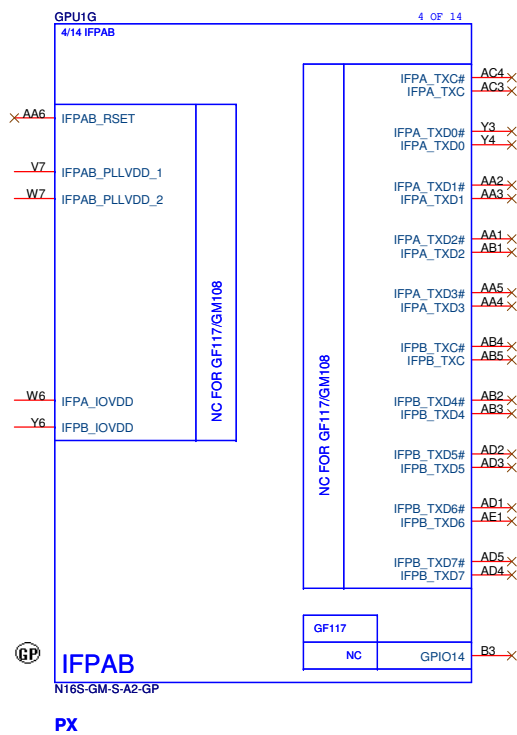
*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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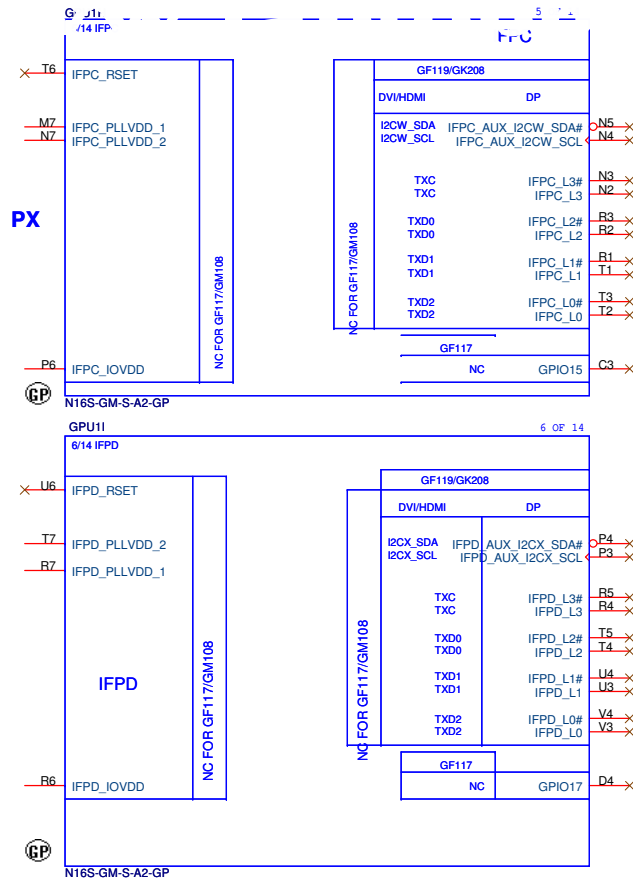
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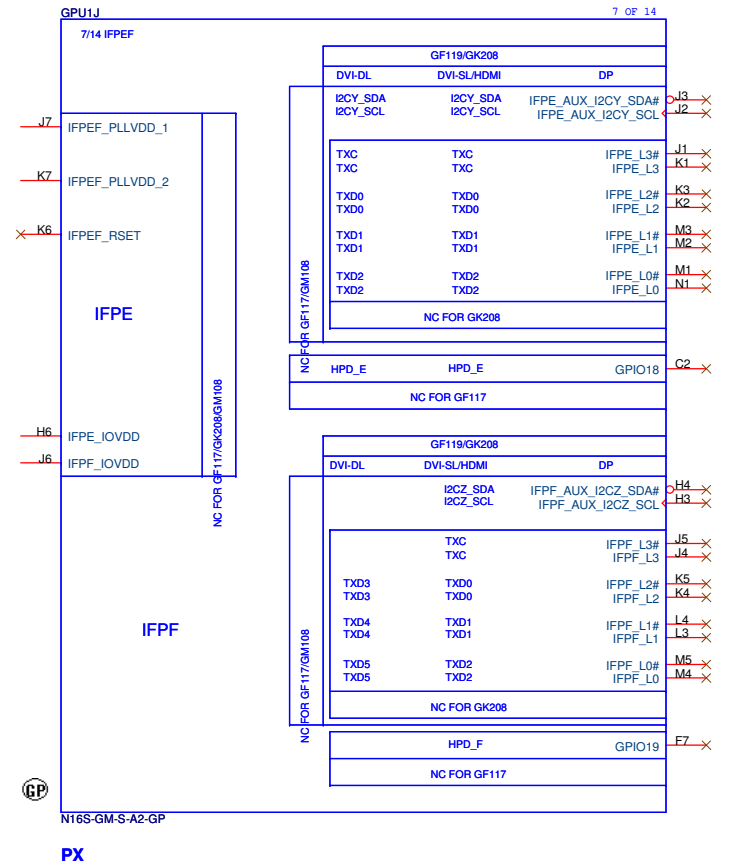
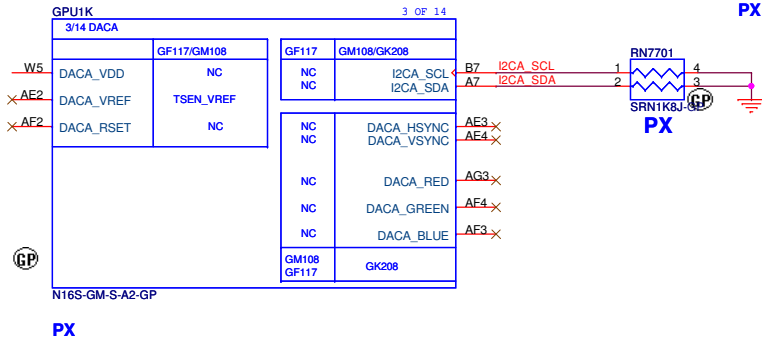
Title		
G-SENSOR		
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Sheet 69 of 106		



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<p>Title GPU (DIGITALOUT)</p>		
Size A3	Document Number Brook BH	Rev -1M
Date: Thursday, February 05, 2015	Sheet 77 of 106	

81.82,83,84 FBA_D[83:0]

FBA_D0

FBA_D1

FBA_D2

FBA_D3

FBA_D4

FBA_D5

FBA_D6

FBA_D7

FBA_D8

FBA_D9

FBA_D10

FBA_D11

FBA_D12

FBA_D13

FBA_D14

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FBA_D47

FBA_D48

FBA_D49

FBA_D50

FBA_D51

FBA_D52

FBA_D53

FBA_D54

FBA_D55

FBA_D56

FBA_D57

FBA_D58

FBA_D59

FBA_D60

FBA_D61

FBA_D62

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FBA_D311

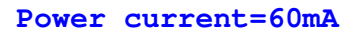
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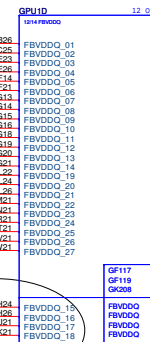
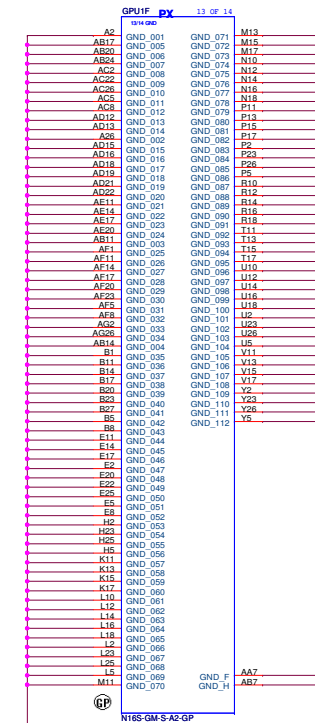
FBA_D314

FBA_D315

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GR28-64 / G82-64	4.7 μ F X65	0403	10	10	Under GPU
	1 μ F X65	0402	4	4	Under GPU
	47 μ F XSR	0805	1	1	Near GPU
	22 μ F XSR	0805	1	1	Near GPU
	4.7 μ F XSR	0805	5	5	Near GPU
	330 μ F POS	7343	1	1	Near GPU ESR < 6 m Ω



GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64/GB2-64 DDR3	0.1µF	X7R 0402	2	Under GPU
	1µF	X7R 0603	2	Under GPU
	4.7µF	X6S 0603	2	Under GPU
	10µF	X5R 0805	1	Near GPU
	22µF	X5R 0805	1	Near GPU

[illegible]

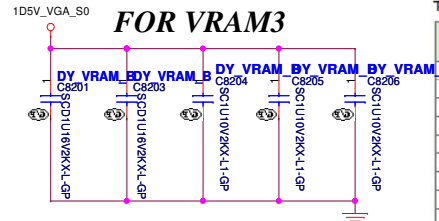
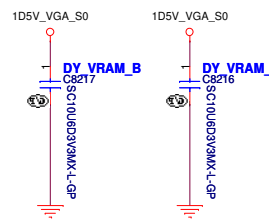
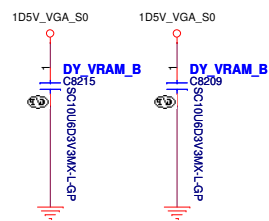
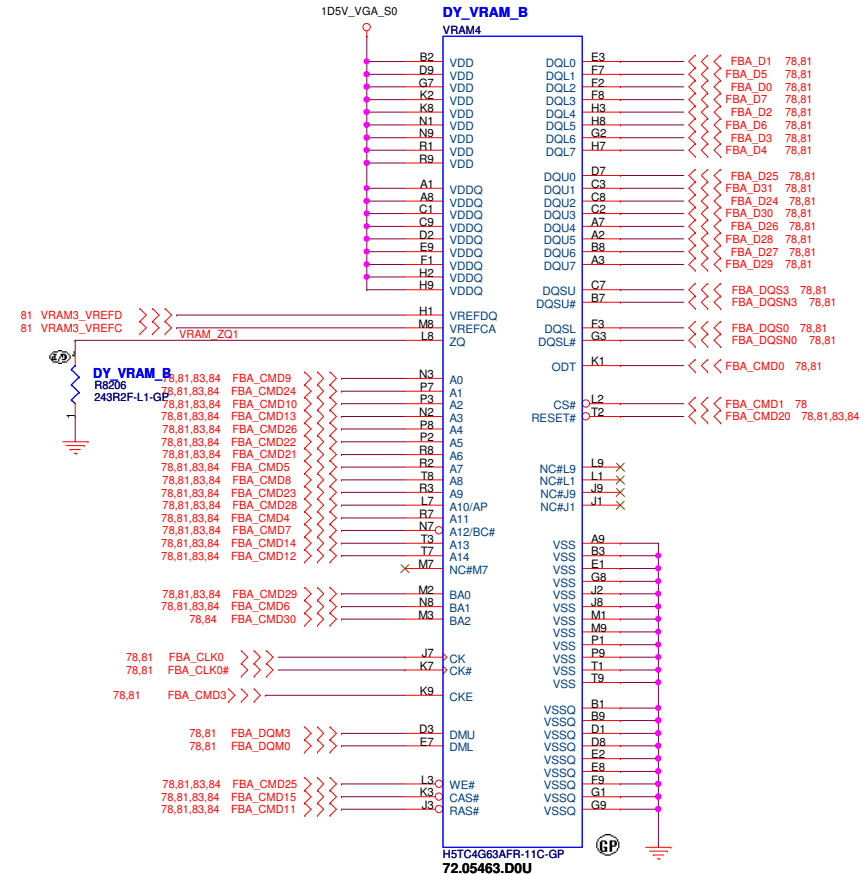
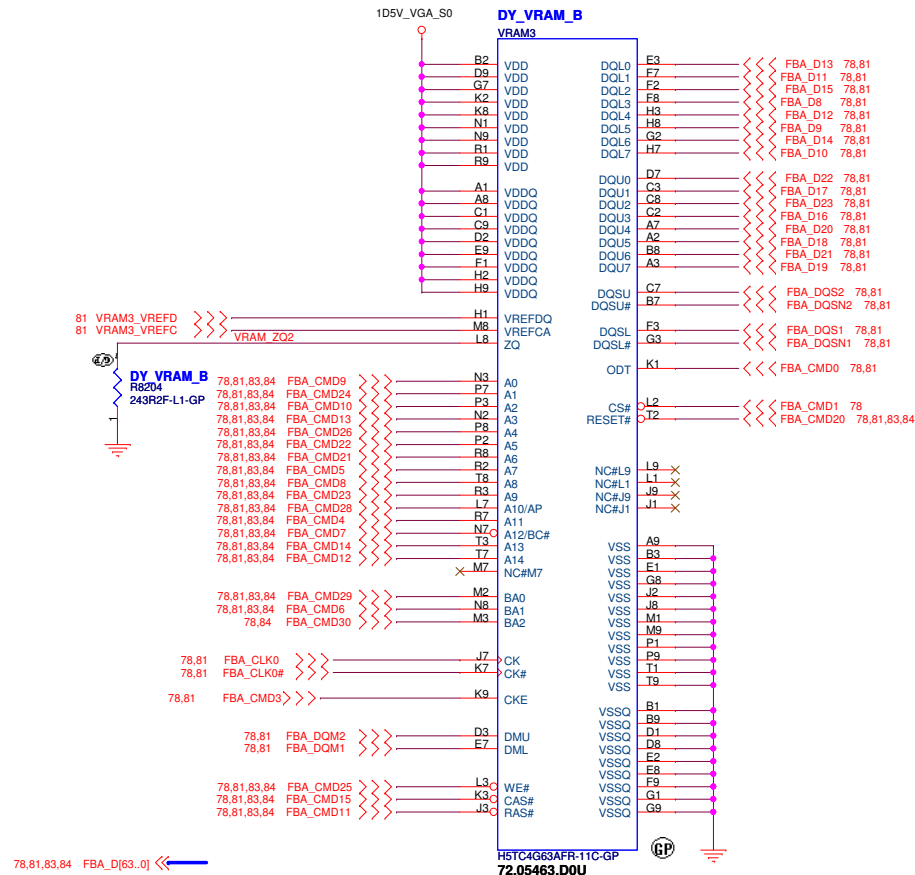
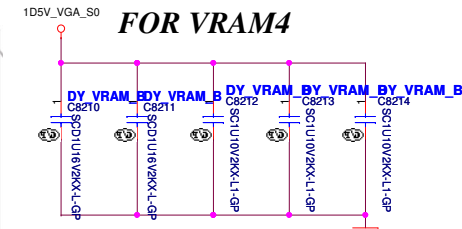


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDDQ/Q Combined					
0.1 μ F	X7R	0402	2		Under DRAM
1.0 μ F	X7R	0603	4		Under DRAM
10 μ F	X5R	0805	0		Close to DRAM
FBVDDQ/Q Separate					
0.1 μ F	X7R	0402	4	2	Under DRAM
1.0 μ F	X7R	0603	3	1	Under DRAM
10 μ F	X5R	0805	0	0	Close to DRAM
Note: *Location is close to DRAM, for clamshell mode.					

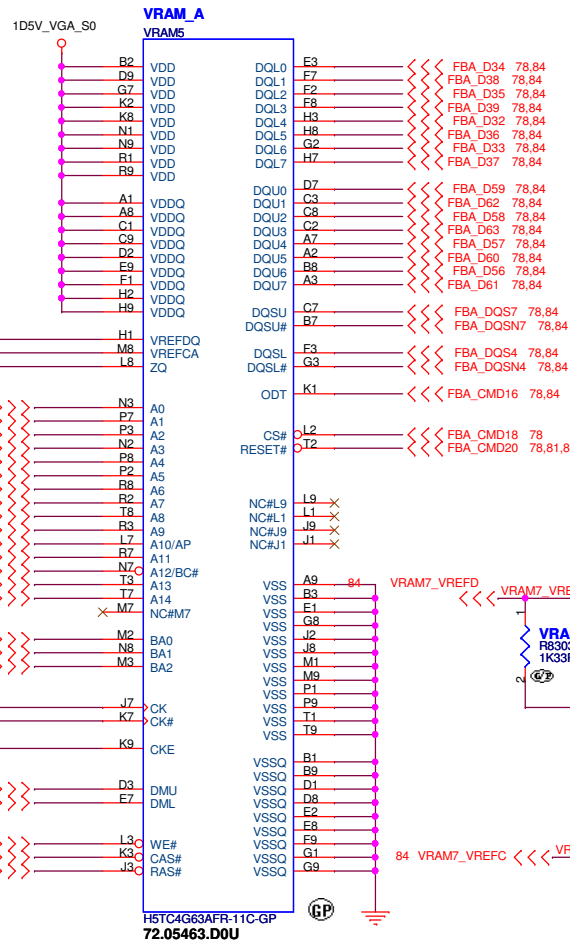
Note: *Location is close to DRAM for clamshell mode.



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
GPU-VRAM3,4 (2/4)			
Title	Document Number	Rev	
Size Custom	Brook BH	-1M	
Date: Wednesday, February 04, 2015	Sheet 82	of 106	



FOR VRAM5

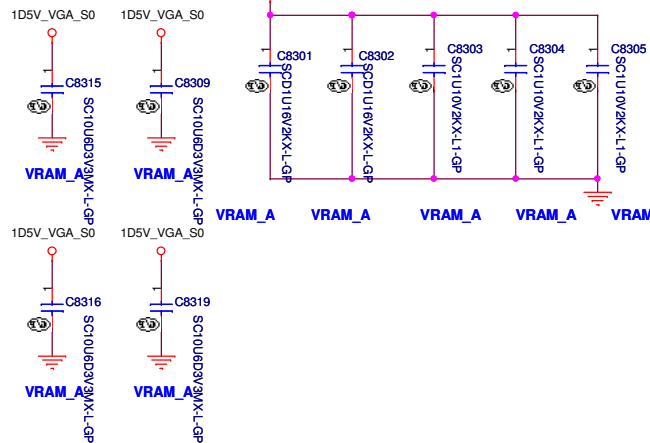
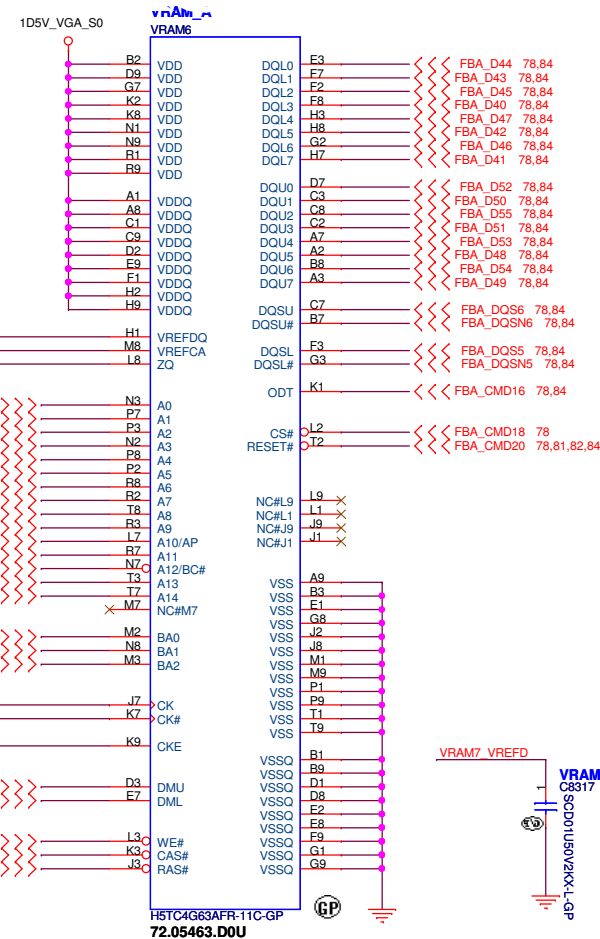


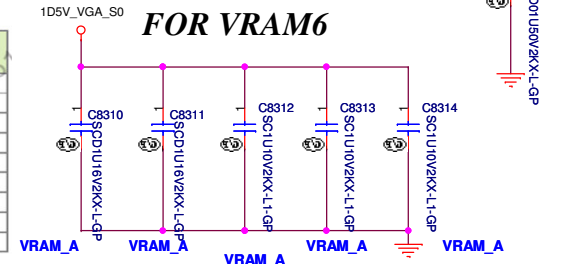
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type	Population		
	FBVDDQ	FBVDD	Location
FBVDD/Q Combined			
0.1 μF	X7R	0402	2
1.0 μF	X7R	0603	4
10 μF	X5R	0805	0
FBVDD/Q Separate			
0.1 μF	X7R	0402	4
1.0 μF	X7R	0603	3
10 μF	X5R	0805	0

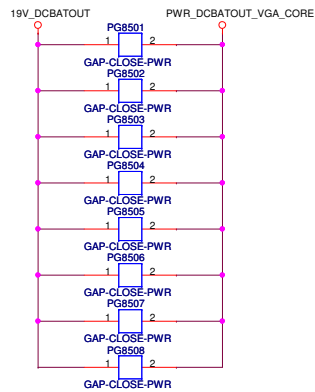
Note: *Location is close to DRAM for clamshell mode.



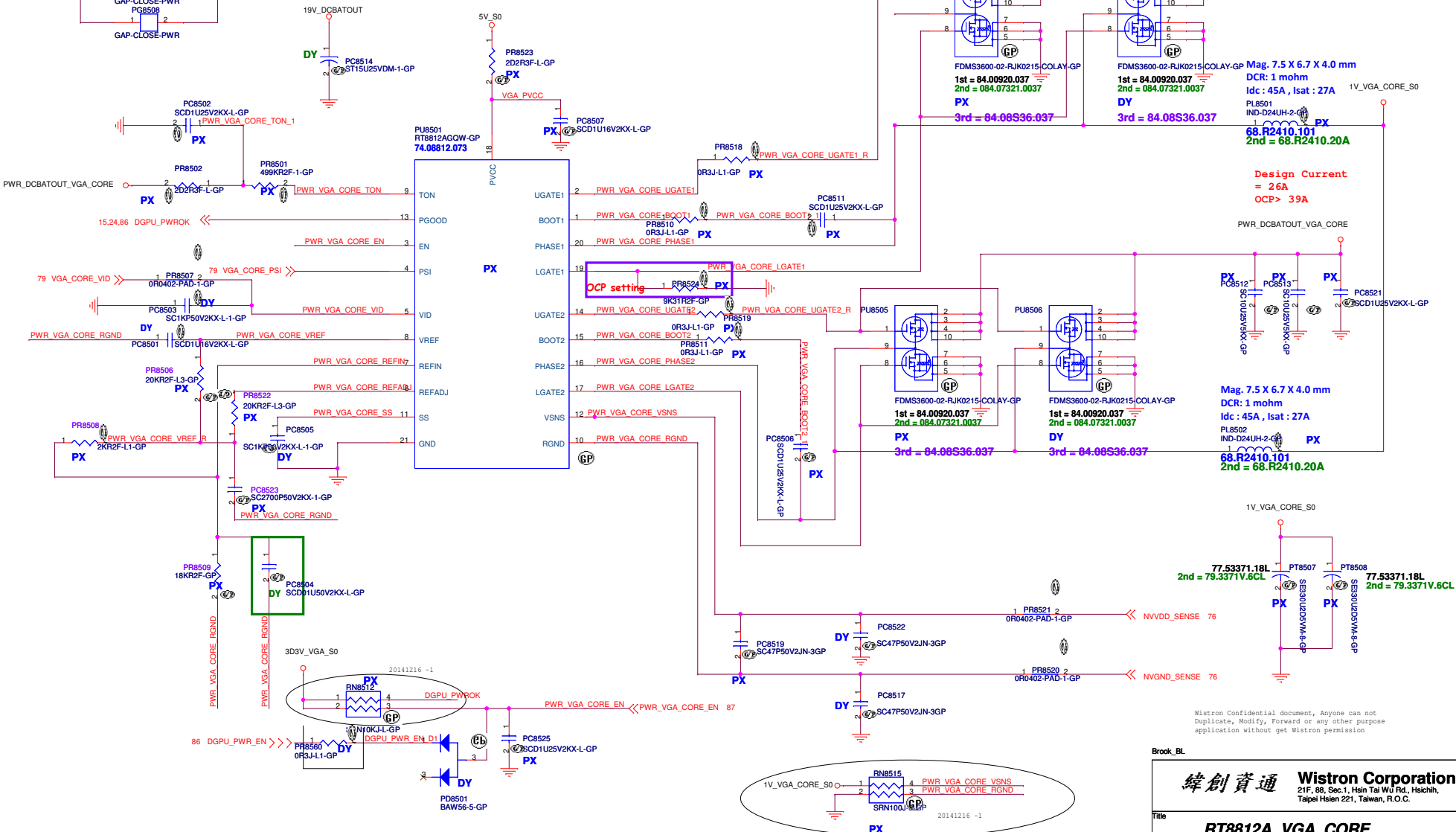
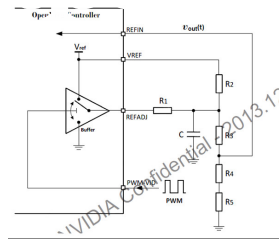
FOR VRAM6



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PWM-VID Specification				
	Config A	Config B	Config C	Config D
Vmin	0.6	0.6	0.65	0.9
Vmax	1.2	1.2	1.45	1.15
Vboot	0.875	0.9	0.9	1.028
Voltage Step Vstep	6.25	6.25	25	12.5
Number of Voltage Levels N	96	96	20	20
PWM Frequency F _{PWM}	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T _{min}	9.26	9.26	74	74
VID Transient Time T	<100	<100	<100	<100
Component Value				
R1 (1%)	KQ 39	20	39	27
R2 (1%)	KQ 39	20	30	7.5
R3 (1%)	KQ 1.5	2	3	0
R4 (1%)	KQ 30	18	24	6.2
R5 (1%)	KQ 1.5	0	3	1.74
C	nF 1.5	2.7	1.8	5.6



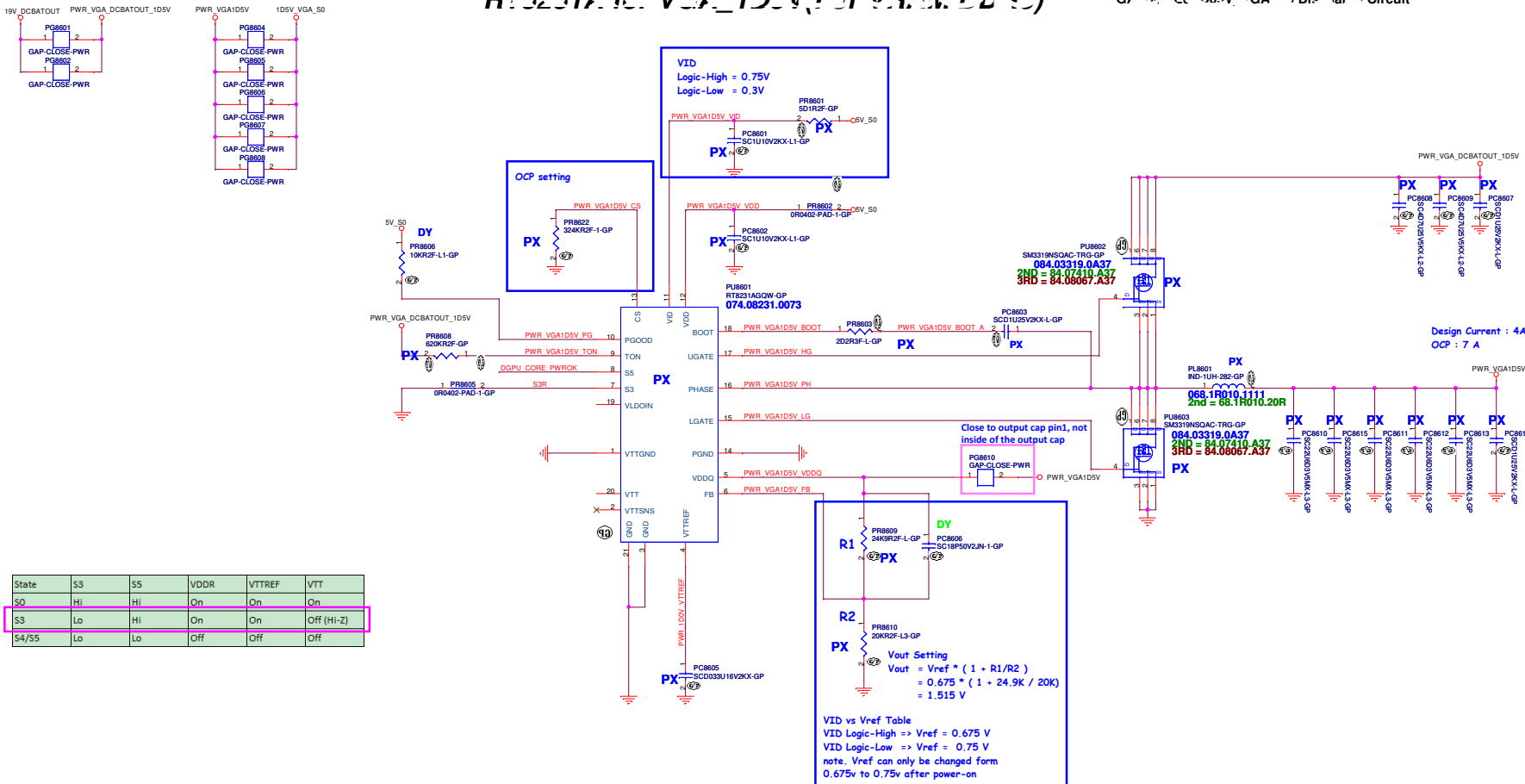
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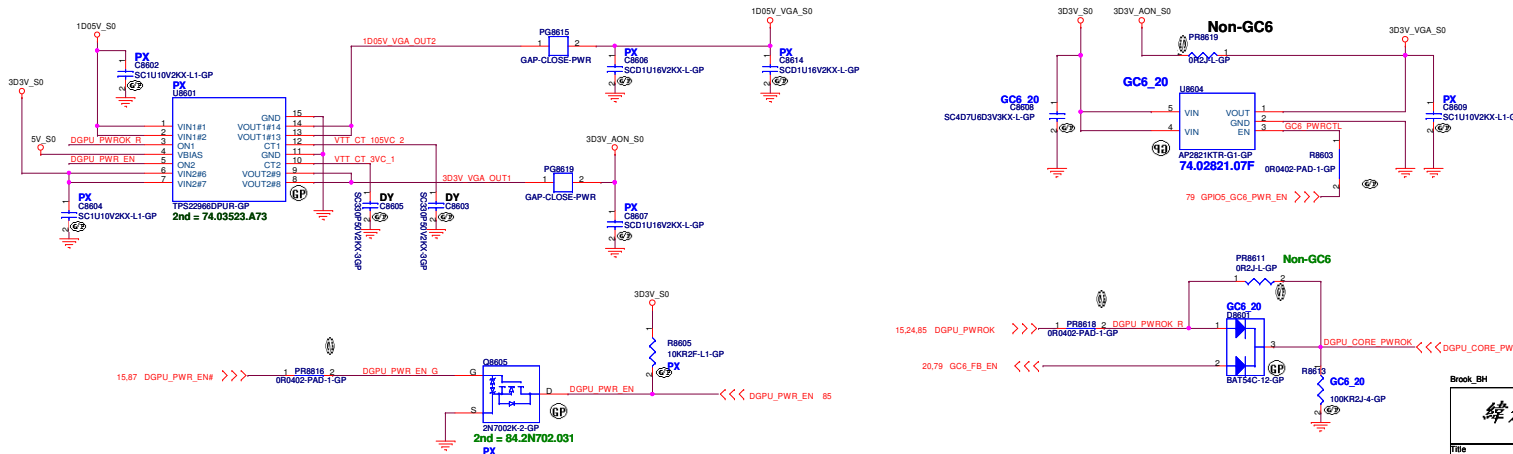
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Title	RT8812A VGA CORE
Size	Document Number
Custom	Brook BL
Date	Wednesday, February 04, 2015
Sheet	85 of 106
Rev	-1M

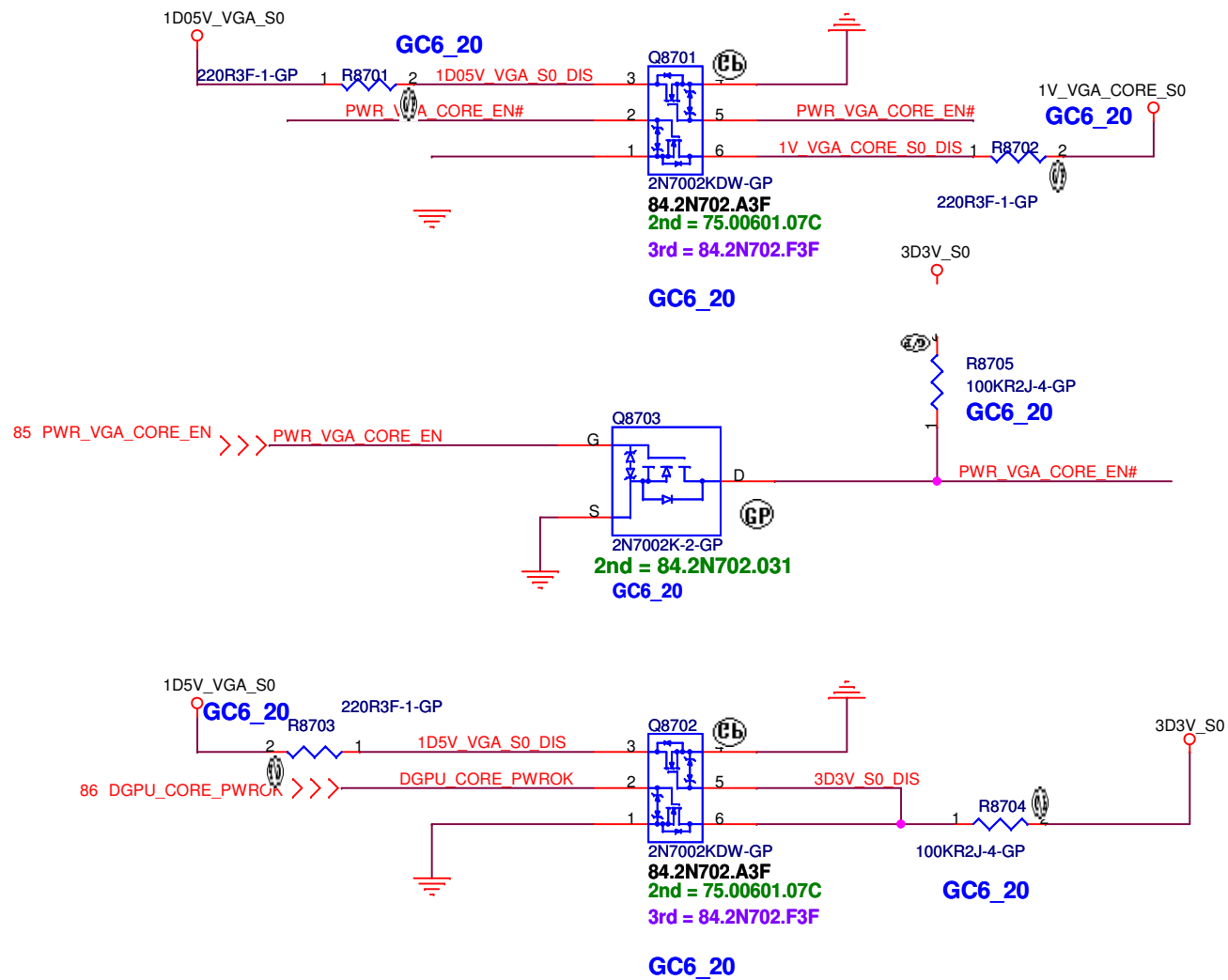
RT8231A for VGA_1D5V (For V3.M.1.D.2)

GPIO, ECU, USB, VGA, Discrete Circuit



3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0





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Title

DISCHARGE

Size
A4

Document Number

Brook BH

Rev

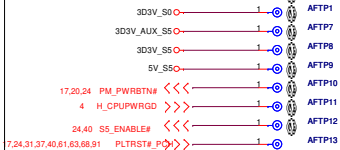
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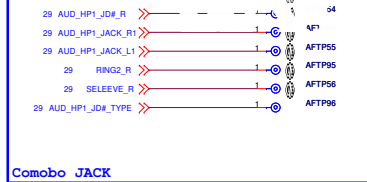
Sheet 87 of

106

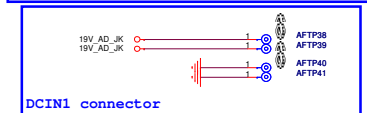
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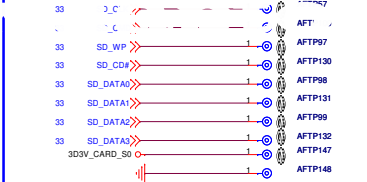
Test Point放在Dimm Door打開可量測處



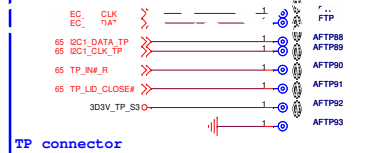
Comobo JACK



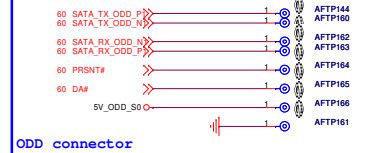
DCIN1 connector



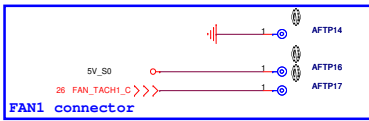
SD Card reader



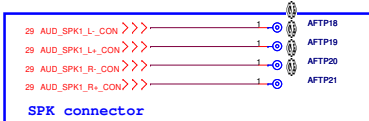
TP connector



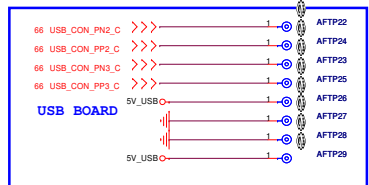
ODD connector



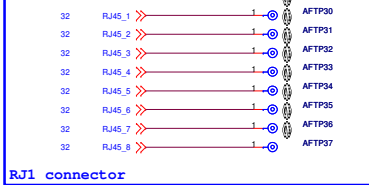
FAN1 connector



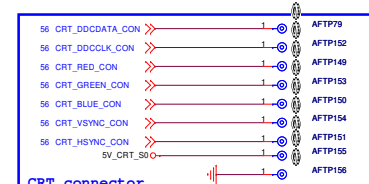
SPK connector



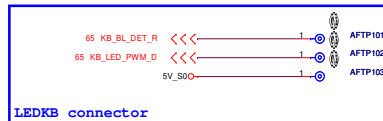
USB BOARD



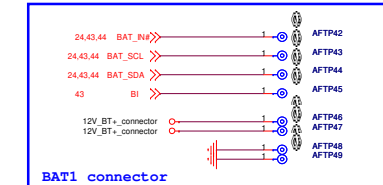
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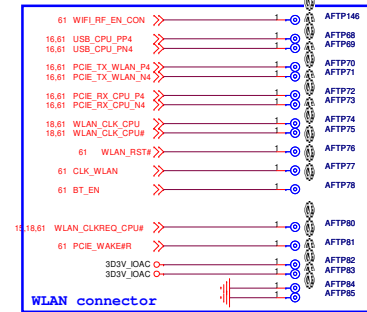
CRT connector



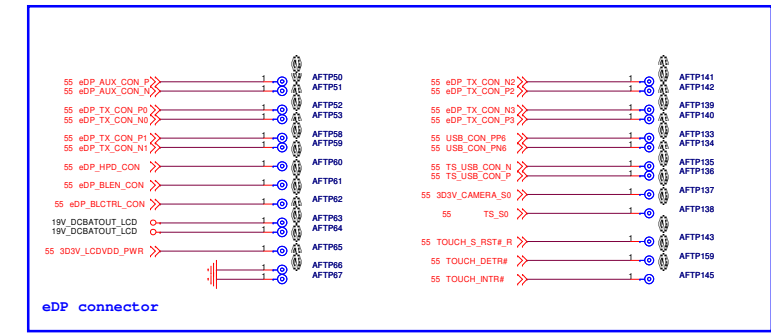
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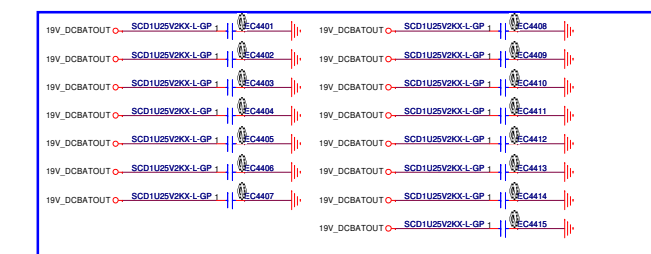
BAT1 connector



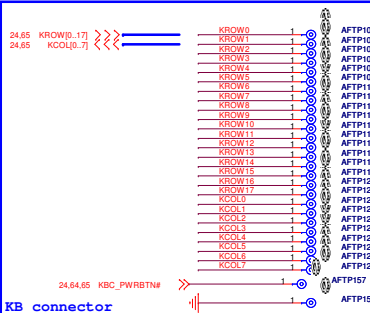
WLAN connector



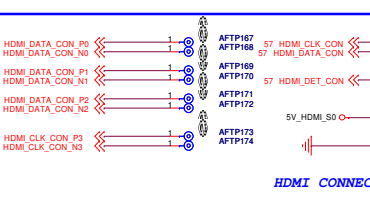
eDP connector



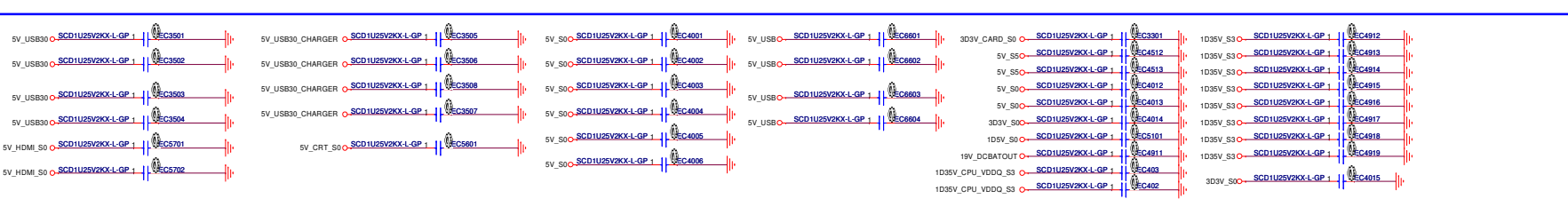
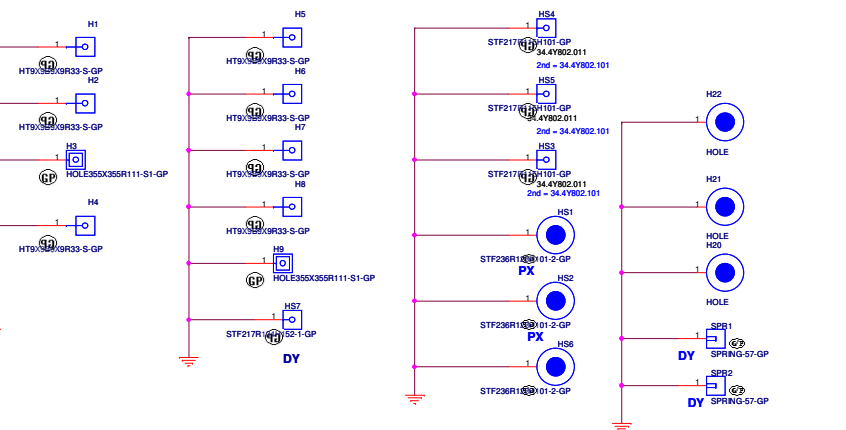
eDP connector



KB connector

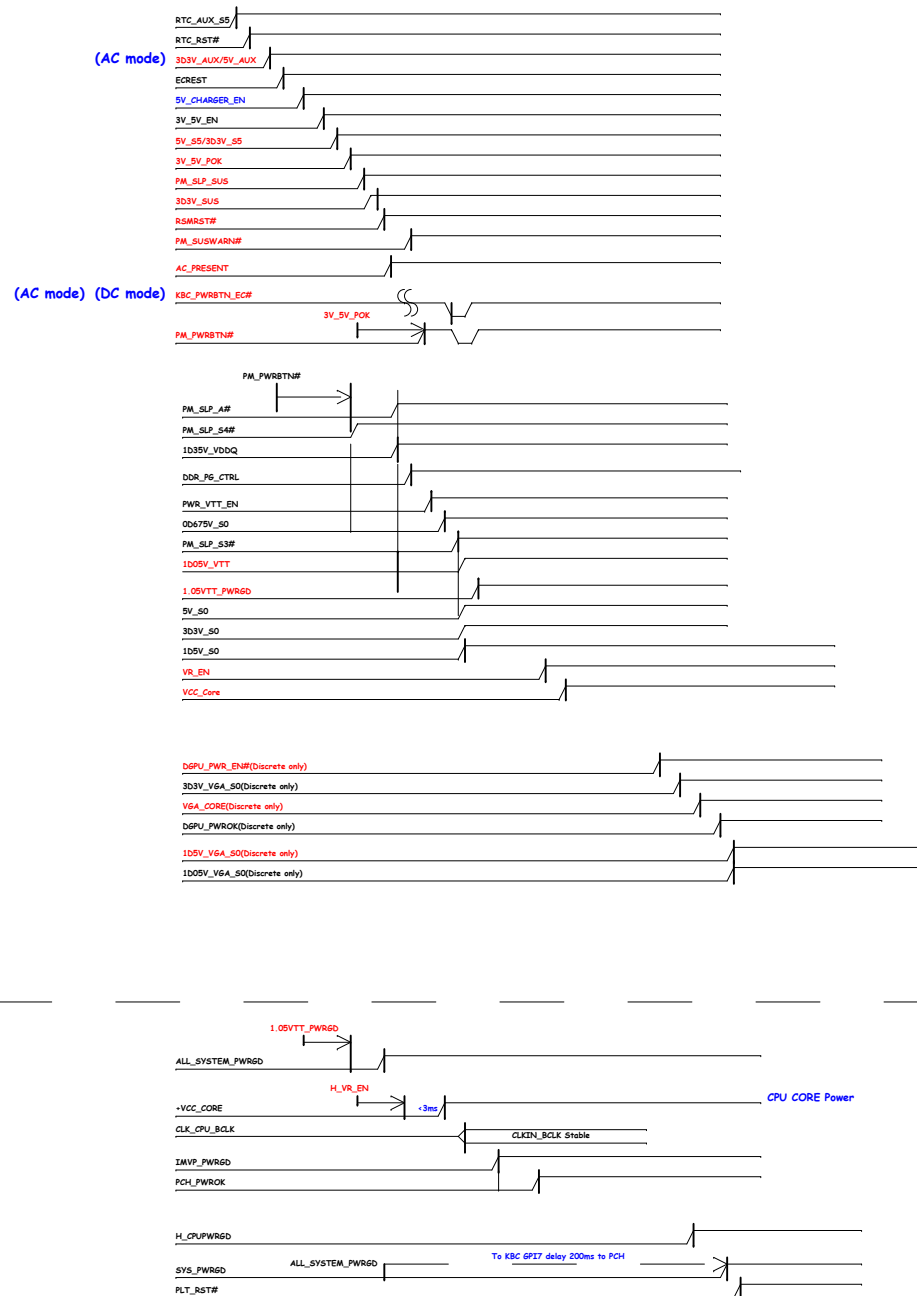


HDMI CONNECTOR

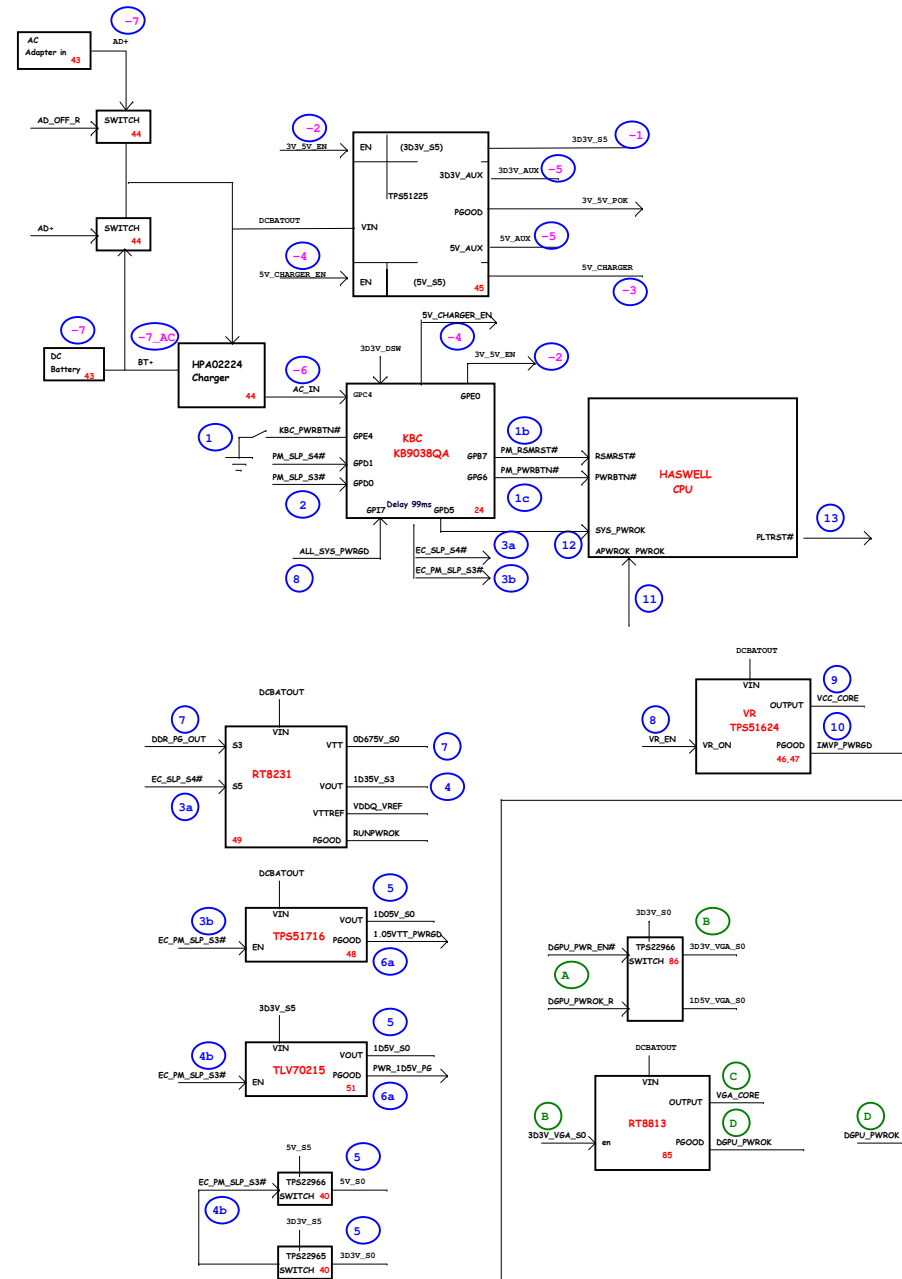


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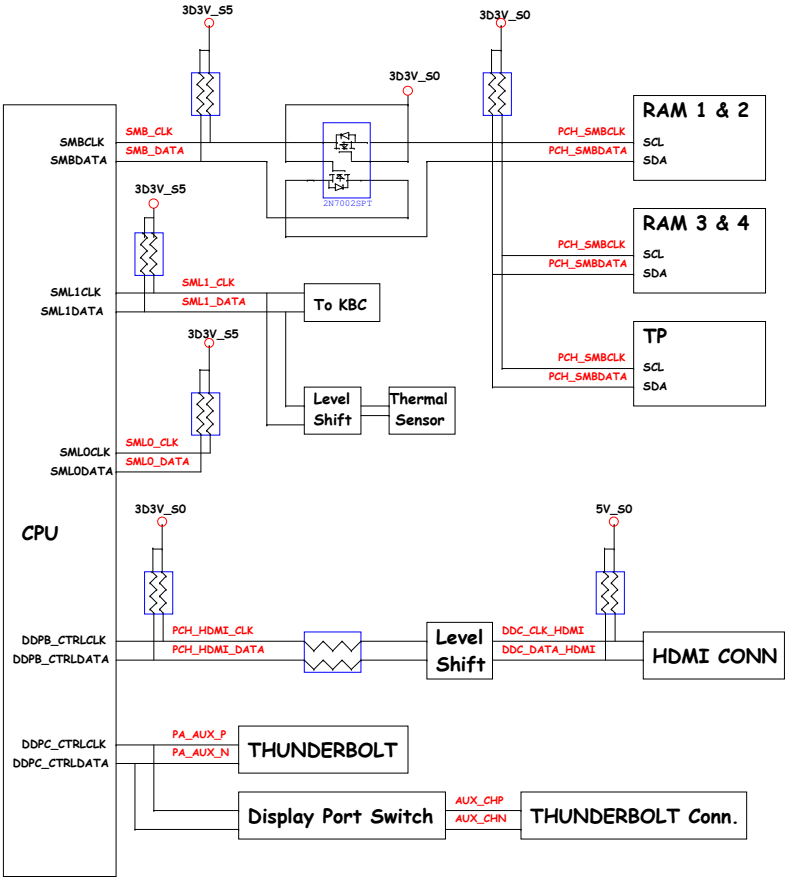
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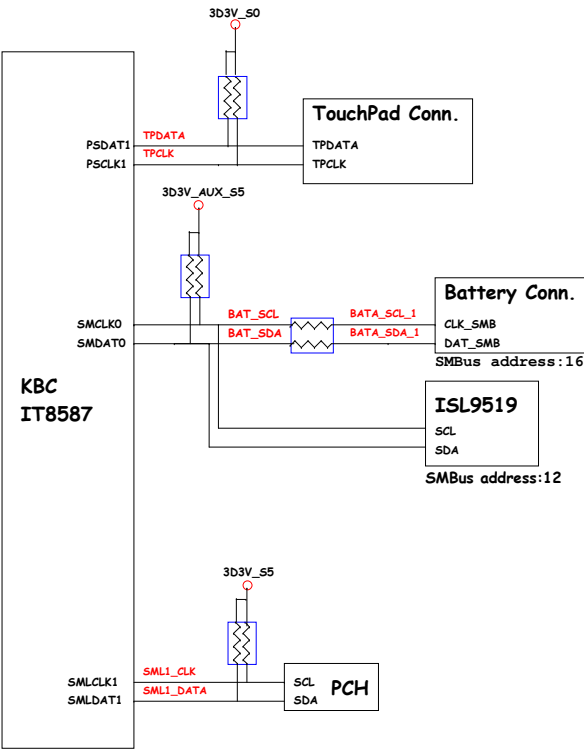
HASWELL POWER UP SEQUENCE DIAGRAM



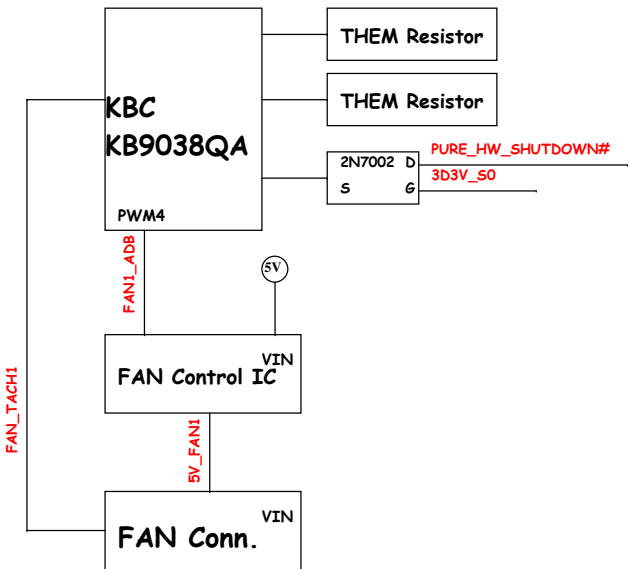
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

